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TAMPERE UNIVERSITY OF TECHNOLOGY

ANTTI KESKINARKAUS

IGBT GATE DRIVER WITH SOFT TURN-OFF FUNCTION

Master of Science thesis

Examiner: University Teacher Jouko Heikkinen
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ABSTRACT

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The purpose of this thesis research was to develop a new gate driver circuit for IGBT semiconductor switches that are used in frequency converters. Frequency converters are widely used in industry and electrical systems of buildings, including elevators and escalators, for energy efficient speed control of electric motors. The thesis is a part of larger research entity done in Danfoss Drives in order to enhance the short circuit protection of frequency converters. The research was based on existing simulations of the driver, done by another development engineer of Danfoss. The reference material used as background information for the research consisted mainly of academic research articles and the fundamental literature regarding electric converters.

The study consisted of performing further simulations for the driver circuit, building a prototype and performing measurements for it in a high voltage testing environment. The testing environment modelled the main circuit of a frequency converter. The target on the driver development was to achieve short delays, high gate currents and fast output voltage transitions, thus providing flexibility for the application-specific adjusting of the driver. The second section of the research consisted of developing an additional soft turn-off circuitry for the gate driver. Soft turn-off can be used for decreasing the turn-off voltage overshoots over the IGBT switch. Overshoots are caused by turning the IGBT off when a short circuit has appeared in the output of the converter. When using normal turn-off switching procedure for high currents, the momentary overvoltage can exceed the tolerance of the IGBT and cause damage to the converter.

The theoretical section of the thesis includes introducing the main circuit of a frequency converter, the structure and controlling method of an IGBT and its behavior in fault situations. Also the general requirements for a gate driver are presented. The section considering the practical research focuses on the technical solutions of the developed driver and measurement results regarding the driver and the driven IGBT. Additionally, the behavior of the IGBT and the main circuit is studied with different configurations of soft turn-off circuit. For comparability of the driver's performance, an existing driver is introduced and measured for reference.

The developed gate driver reached the targets for the gate current and delays. It reduced the delays caused by the driver by more than 50 % when compared to the reference driver. In turn, chosen gate power supply voltages turned out to be rather low. Also the power rating of the IGBT module in the test setup was significantly lower than what the driver is designed for. The soft turn-off was reducing the turn-off overvoltage even more than expected. According to measurements performed with the final configuration, the overshoots were 82 % lower than when using the normal turn-off.

TIIVISTELMÄ

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Tämän diplomityön tavoitteena oli kehittää aiempien simulointien pohjalta uusi taajuusmuuttajissa käytetyn IGBT-puolijohdekytkimen hilaohjainkytkentä. Taajuusmuuttajia käytetään yleisesti teollisuudessa ja rakennustekniikassa sähkömoottorien pyörimisnopeuden energiatehokkaaseen säätöön. Työ on osa Danfoss Drivesissa toteutettavaa tutkimuskokonaisuutta, jolla pyritään parantamaan taajuusmuuttajien oikosulkusuojausta. Työn taustamateriaali koostui valmiiden simulointitulosten lisäksi pääosin aihetta sivunneista kansainvälisistä tutkimusjulkaisuista sekä alan perusteoksista.

Työ koostui tarkentavien simulointien lisäksi prototyypin rakentamisesta ja mittauksista korkeajännitteisessä testiympäristössä, jolla mallinnettiin taajuusmuuttajan tehonsiirtoon tarkoitettua pääpiiriä. Kehitetyltä hilaohjaimelta tavoiteltiin ohjaimen lyhyttä toimintaviivettä, suuria hilavirtoja, askelmaisesti muuttuvaa lähtöjännitettä ja sillä saavutettavaa laajaa hilajännitteen muutosnopeuden säätöaluetta. Hilaohjaimeen liitetty IGBT:n kollektorivirran hidastetun sammutuksen lisätoiminto muodosti työn toisen osakokonaisuuden. Hidastetulla sammutuksella voidaan madaltaa taajuusmuuttajan moottorilähdön oikosulun poiskytkennän jälkeisiä ylijännitteitä, jotka tavanomaista poiskytkentää käytettäessä voisivat ylittää IGBT:n kestorajat ja aiheuttaa laitevaurioita.

Työn teoriaosuudessa käydään läpi taajuusmuuttajan pääpiirin perusrakenne, IGBT-puolijohdekytkimen rakenne, ohjaaminen ja käytös vikatilanteissa, sekä hilaohjaimelle asetetut yleiset vaatimukset. Työn käytännön toteutusta käsittelevä osio keskittyy hilaohjaimen teknisten ratkaisuiden esittelyyn sekä mittaustulosten läpikäyntiin hilaohjaimen ja ohjatun IGBT:n osalta. Lisäksi tutkitaan IGBT:n käyttäytymistä erilaisilla hidastetun sammutuksen komponenttiarvoilla ja pohditaan perusteluja sopivien arvojen valinnalle. Hilaohjaimen kyvykkyyden arvioimiseksi esitellään olemassa oleva referenssikytkentä, johon tutkitun ohjaimen toimintaa verrataan.

Kehitetty hilaohjain saavutti sille asetetut tavoitteet hilavirran ja viiveiden osalta, lyhentäen ohjainkytkennästä aiheutuvan viiveen alle puoleen referenssikytkennän viiveestä. Toisaalta ongelmaksi havaittiin testausjärjestelmään valittu matalahko ohjaimen käyttöjännite sekä ohjainkytkennän alhainen kuormitus. Mittausjärjestelmään valittu IGBT-moduli on merkittävästi pienempitehoinen hilaohjaimen mahdollisiin tuleviin käyttökohteisiin nähden. Hidastettu sammutus alensi poiskytkennän jälkeisiä ylijännitteitä jopa odotettua enemmän, saavuttaen lopulliseksi valitulla toteutuksella 82 % matalamman ylijännitetason kuin normaalilla poiskytkennällä.

PREFACE

This Master of Science thesis is written for Vacon Ltd, which is a part of Danfoss Drives. The basic idea for the thesis was developed by M.Sc. Paavo Merilinna in the form of preliminary schematics and simulations. The research process and thesis were coordinated by M.Sc. Janne Pakkala and examined by University Teacher Jouko Heikkinen.

I want to thank all the parties that have taken part in this work by attending meetings and reviews as well as offering ideas and support, but also by encouraging me to focus on the core idea. Especially I want to thank my most important sources, our experienced designers Paavo Merilinna and Jari Koljonen, for the practical knowledge and support gained through the work. Paavo offered the topic and gave his support throughout the process, while Jari introduced the requirements for the device's capability and helped a lot with the final measurements. Many thanks also for my coordinator, Janne Pakkala, who has not only made working with this thesis possible, but kept my side by ensuring the continuity of my career.

Thanks also go for my examiner, Jouko Heikkinen, for the willingness of taking part to the finalizing of my studies. It has been several years of cooperation now, which has left me a strong basis and interest for developing myself further in my career. You have been a great support for that.

Finally, I want to thank my family for the support and my friends for the shared years of studies. And thanks for my dear Noora for believing in me through this process.

Tampere, 29.5.2016

Antti Keskinarkaus

CONTENTS

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LIST OF SYMBOLS AND ABBREVIATIONS

IGBT	Insulated Gate Bipolar Transistor
BJT	Bipolar Junction Transistor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
CPLD	Complex Programmable Logic Device
GST	Gate Soft Turn-off
PCB	Printed Circuit Board
SMD	Surface Mounted Device
THD	Through Hole Device
VSI	Voltage-source inverter
ESR	Equivalent Series Resistance
ESL	Equivalent Series Inductance
PE	Protective Earth
PWM	Pulse-width modulation
t	Time
V_{CE}	Collector-emitter voltage of an IGBT
V_{GE}	Gate-emitter voltage of an IGBT
$V_{GE(TH)}$	Gate-emitter threshold voltage of an IGBT
$V_{DC\text{-}LINK}$	DC-link voltage
V_{DC}	Constant voltage
V_{AC}	Alternating voltage
V_{TO}	Turn-off overshoot voltage
$R_{G,INT}$	Internal gate resistor of an IGBT
$R_{G,ON}$	External turn-on gate resistor in a gate driver circuit
$R_{G,OFF}$	External turn-off gate resistor in a gate driver circuit
$C_{G,AUX}$	Auxiliary gate capacitor in a gate driver circuit
C_{GE}	Parasitic capacitance between IGBT's gate and emitter
C_{GC}	Parasitic capacitance between IGBT's gate and collector, "Miller capacitance"
L_S	Stray inductance of a circuit
I_C	Collector current of an IGBT
I_D	Current through the free-wheeling diode inside an IGBT module
E_{ON}	Turn-on switching loss of an IGBT
E_{OFF}	Turn-off switching loss of an IGBT
Q_G	Gate charge
$Q_{G,AUX}$	Charge of auxiliary gate capacitor
σ	Standard deviation
U, V, W	Output phases in a three-phase frequency converter. Used only when referring to the main circuit of the converter.

1. INTRODUCTION

The purpose for this study was to develop a new gate driver circuit for controlling the insulated gate bipolar transistor (IGBT) switches used in frequency converters. The developed gate driver was to be capable of handling high momentary currents combined with short delays in the control chain and ability to work with only one gate-connected two-sided supply. This would lower the costs of the final device. The new driver was planned to be an alternative for the current designs in the high-power industrial converters.

Another feature for the driver circuit was to accommodate a circuit for performing a slowed turn-off switching, called *soft turn-off*, which would be used in decreasing the overvoltage caused by switching in short circuit situations. The overvoltage is caused by performing a normal turn-off procedure to a heavy load current that has increased fast due to low inductance of a short circuit. Performing a normal turn-off causes a rapid decrease in the IGBT's collector current, which again induces a momentary voltage in the stray inductances of the main circuit of frequency converter. Since this voltage is summed up with the original steady-state voltage of the converter's DC-link, the voltage stress of the IGBT is increased. The overvoltage can in certain situations increase to a level which exceeds the IGBT power module's withstanding limits, leading to a failure of the module and the whole device. Using a soft turn-off lowers the rate of change of IGBT's current, which helps in maintaining the overvoltage on an acceptable level. A simplified functional block diagram of the prototyping setup is introduced in Figure 1. The narrow arrows represent low-voltage control signals while the wide arrows are used for visualizing currents in the simulated main circuit.

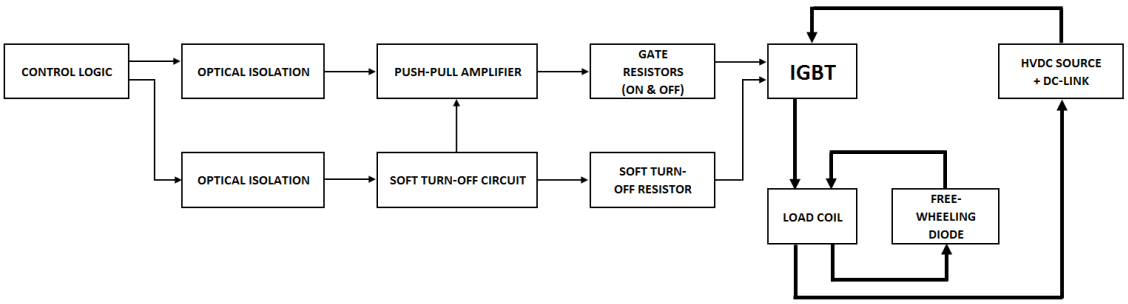

Figure 1. *A simplified operational block diagram of the developed prototype*

The failures caused by overvoltage in short circuit situations are an identified risk, and it has been studied widely as came out when going through the references. However, there was no common solution for the issue in the company's current design catalogue. It was regarded advantageous to perform a research in order to find a working solution that

would be easy to scale. It would be later complemented with a fast overcurrent recognition circuitry, placed on the control system in addition to the normal current measurement.

The work consisted of simulating and designing the schematics, drawing the layout and routing for the prototype board, building a high-precision control logic for the test setup, tuning the driver's operation by adjusting component values on the complete device and finally verifying the board's capability by using a high voltage test bench. The basis for the schematics and simulations was got ready from the archive of Senior R&D Design Engineer Paavo Merilinna, but there was still plenty of work to be done before the design reached its final appearance.

The research process began by completing the unfinished parts of the schematics according to simulations and converting the simulation schematics of Appendix I to the printed circuit board design software. Shortly after that the layout was drawn and the planning work for verifying the board got started. Since most of the currently used drivers were developed for past projects, the knowledge about their verification and evaluation criteria was not readily available. In collective meetings with both electronics and main circuit designers, a list of the needed measurements was created. It was later replenished after detecting unexpected operation. The main focus in measurements was in finding answers for the following questions:

- What are the operational delays of the gate driver circuit?
- What is the maximum output current the gate driver can provide?
- What is the highest steady-state voltage that the driver can supply for the gate without letting the push-pull stage transistors enter into hard saturation?
- What are the optimal values for gate discharging resistor and capacitor in the soft turn-off circuit?
- What is the effect of soft turn-off for the turn-off overvoltage?

After reviewing the design, the manufacturing of the board was initiated and the work was focused on modifying an existing control system's hardware logic description to support the timer-triggered soft turn-off test function. The logic controller is located on an additional prototyping board that is connected to the interface part of the driver prototype.

The measurements in a low voltage test setup were started immediately after receiving the boards and assembling the last missing components. After verifying that the control circuit and logic are operational, the measurements continued gradually towards the output of the driver. After performing modifications, it was verified that the upgrades had not affected backwards in the control chain. The same was done for the soft turn-off circuitry. As the driver was considered ready, the IGBT's switching characteristics were investigated in both normal and short circuit situations in a high voltage test bench. As the final step, the IGBT was stressed in turn-off overshoot tests.

The theoretical background of frequency converters, IGBT switches and gate drivers is presented in Chapter 2 to introduce the phenomena and to justify the decisions made in the design. The main focus is put on the IGBT's behavior in switching under normal and short circuit conditions and the operation of gate driver circuits. In Chapter 3, the built prototype, measurement arrangements and methods of data handling are presented. The results are presented in Chapter 4. In Chapter 5, the conclusions are introduced with the discussion of the reliability and the coverage of the study. Also some future actions needed for taking the design into production are suggested.

The original oscilloscope screen captures, large tables, the schematics and the layout images of the prototype are mainly included in the appendixes. Additionally, some findings and minor topics that affected the research but were not considered essential for the thesis can be found there.

2. THEORETICAL BACKGROUND

In this section, the essential theoretical background for understanding the environment and operation of the studied IGBT gate driver is introduced. A top-down approach is used, starting from the introduction of a frequency converter and its characteristics related to the studied design, and then continuing to the controlled switching component, IGBT. Finally, the operation and characteristics of a gate driver circuit are discussed in detail.

2.1 Frequency converters

Frequency converter is an electronic device that is used to drive AC motors at a variable speed. Modern frequency converters make use of high power semiconductor switches and PWM modulation in their operation. The need for a variable AC frequency arises from the characteristic behavior of an induction motor; the axle rotation speed is dependent to the frequency of their supply voltage. Since industrial motors are mainly powered from the electric grid, the axle frequencies of the motors are not effectively adjustable if they are connected straight to the grid. [8]

There are some different topologies for a frequency converter, but in this scope only converters with a pulse-width modulation (*PWM*) controlled, three-phase, voltage-source inverter (*VSI*) as an output bridge are studied. Using PWM modulation lowers the need for filters and increases the controllability when compared to six-step modulation. [8]

2.1.1 Main circuit

The main circuit of a VSI-based frequency converter consists of an input bridge, DC link capacitor and an output bridge, which in this scope is considered to be consisting of IGBT modules. In addition, there may be filters, contactors, charging and braking components, fuses and other external equipment, but introducing them is not needed for understanding this study. A simplified circuit diagram of the main circuit is presented in Figure 2.

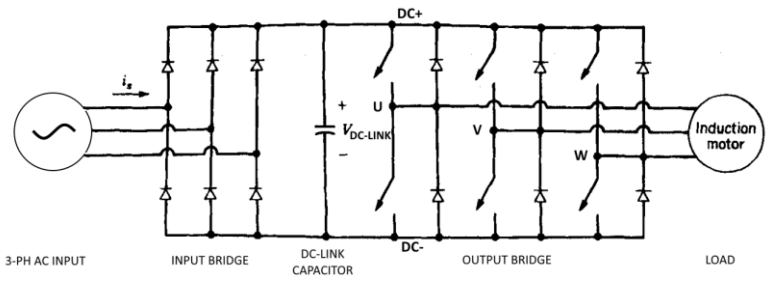

Figure 2. *A simplified main circuit of a frequency converter. Adapted from [16].*

The structure of the input bridge varies with the intended use and power class of the converter. It can be built with diodes, as in Figure 2, or with thyristors or IGBTs, gaining in different levels of control over the input current and voltage waveforms. Input can be supplied from a one- or three-phase grid or from a common DC bus. [8] The effect of the input bridge structure to the gate driver circuit is negligible, since the DC-link voltage in this study is considered constant with the exception of studied switching overshoots.

The DC-link capacitors are used as an energy reservoir. The rectified voltage from the three-phase diode input bridge has some ripple, whose frequency is six times the grid frequency. To be able to create a clean, non-distorted waveform for the output voltage and to limit the route of high-frequency pulse current caused by the PWM modulation of the output bridge, relatively large capacitors are used in the DC-links of VSI-based frequency converters. Additionally, the DC-link capacitors decrease the voltage overshoots caused by output bridge switching. The capacitors have to fulfill the requirement for the rectified voltage level with a margin. This may cause a need for connecting several capacitors in series to meet the sufficient voltage rating. However, in this document the capacitor assembly is considered to be a single capacitor and it is referred as *DC-link capacitor*, taking no stand for the structure. The negative pole of the DC-link capacitor is referred as *DC-*, while the positive is referred as *DC+*.

For this study, the most significant part of the main circuit is the output bridge. It is used to convert the relatively constant DC-link voltage to AC voltage with a variable frequency and amplitude. To gain a flexible and efficient control over the output voltage, IGBTs or IGBT modules consisting of several IGBTs are used. The number of used switches is mainly defined by the requirements for the output current and DC-link voltage. In a three-phase bridge, six IGBT switches are normally used. They are arranged in pairs, one pair for each *output phase leg*. A phase leg consists of one high-side and one low-side IGBT. High-side IGBTs are located between the output phase and the DC+ while the low-side IGBTs are between DC- and the corresponding output phase. The output phases are commonly named as *U, V* and *W*. As can be noticed in Figure 2, in parallel with each IGBT in the output bridge, there is *a free-wheeling diode*. Free-wheeling diodes are needed to offer a reversal current path when an inductive load is driven by the converter. During the conduction of the corresponding IGBT they are reverse biased.

Only one switch of a pair is driven conductive at once, causing the corresponding output phase voltage to be switched to either DC- or DC+ potential. A principled output waveform generating between output phases U and V is presented Figure 3 and marked as v_{UV}. Simultaneous conduction of both high- and low-side IGBTs would cause an intense current from the DC+ bus to the DC- bus through the IGBT phase pair. Such situation is referred as *short cross conduction* [4]. Therefore is has to be made sure that the high- and low-side gate drivers do not receive driving signal simultaneously. Additionally, it has to

be taken into account that the turn-off time for an IGBT may be significantly longer than the turn-on time. Also the component tolerances and the structure of the signal chain has to be taken into account; if the low-side drivers are not isolated by optocouplers, their delay may be significantly shorter than the high-side drivers'. The interval when neither of the IGBTs is turned on is referred as *dead time* or *interlock delay time*. During dead time, the load current is commuted from the high-side IGBT to the low-side free-wheeling diodes and vice versa. The commutation depends on the load current direction before the switching. The minimum dead time is defined as the difference between the maximum total turn-off time and the minimum total turn-on time [4]. The dead time is normally handled by the control unit of the converter.

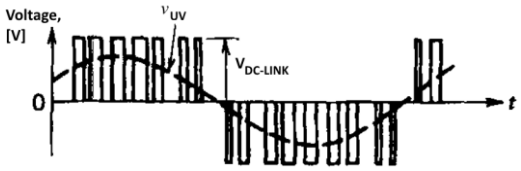

Figure 3. *Output voltage waveform generation. Adapted from [16].*

In modern frequency converters, a modulation scheme called *space vector modulation* is often used. Without going into a deep analysis on the modulation scheme, it can be simplified that the IGBTs are controlled with a logical PWM signal, causing one IGBT from each pair to be conductive at once. [8] The modulation frequency is in the order of kHz.

2.1.2 Non-idealities of main circuit

The real main circuit components have also secondary qualities: the DC-link capacitors, buses and switching components have a certain amount of series resistance as well as parasitic capacitance and stray inductance. Additionally, the IGBTs and free-wheeling diodes do not represent an ideal short circuit when conductive and the switching does not take place infinitely fast like mentioned in the end of the previous chapter. For this study, the stray inductance of DC-link capacitors, buses and the IGBT's bond wires have the major effect. The equivalent circuit of the main circuit with the stray inductances is included in Figure 4. The load is modelled as an inductance. [11]

To decrease stray inductance of the main circuit, special low-inductance capacitors, called *snubber capacitors*, are commonly used between DC+ and DC-. They are placed as close to the IGBTs as possible, often one for each IGBT pair. They reduce the effect of stray inductances L_{DC+}, L_{DC-} and L_{ESR}. Their capacitance is significantly lower than a DC-link capacitor's, being normally in the order of 100 nF. [3] By reducing the stray inductance of the main circuit, the overvoltage caused by high di/dt in the short circuit situations will be decreased. [5][8] R_{ESR} represents the equivalent series resistance of DC-link capacitor.

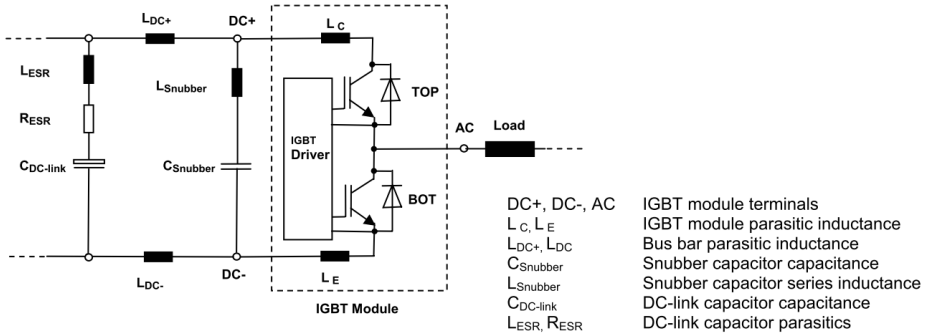

Figure 4. *Equivalent circuit of switching a low-side IGBT with stray inductances L_x included [11]*

Another meaningful phenomenon is the *reverse-recovery time, t_{rr},* of free-wheeling diodes. During commutation of current from the diode to the IGBT, the diode has to change its state from conductive to non-conductive rapidly. As this cannot happen infinitely fast in a real component, the current continues flowing in reverse direction for a certain time interval, t_{rr}, after the polarity of voltage has already changed. This happens especially when an inductive load is connected. The di/dt defined by the switched load and switching component affects the reverse-recovery current value. Therefore, the reverse-recovery time has to be taken into account when defining the used turn-on gate resistor values for the IGBT's gate driver. Neither the turn-on is ideal. As for the turn-off, the diode needs time to change its state from non-conductive to conductive. If the change in applied external voltage is fast, the forward voltage overshoot can be significant. The reverse-recovery time and current waveform are diode-specific features. [16]

2.2 Insulated Gate Bipolar Transistor (IGBT)

In low power applications, bipolar junction transistors (also known as *BJTs*) and MOSFETs are commonly used and they both have their own special application areas. MOSFETs have faster switching speeds especially when comparing turn-off characteristics, but BJTs perform better when large load currents are to be controlled due to their lower on-state losses. This is highlighted when components with high blocking voltages are compared. IGBTs were developed to combine the best characteristics of these two transistor types in terms of delivering high power efficiently. [16]

In general, IGBTs are controlled by applying a voltage on their gates. As a distinction from MOSFET and BJT, IGBTs are designed to be used solely as switches. Linear use of IGBTs in their normal operational environment would cause excessive thermal losses. IGBTs work in linear operating conditions only during switching and under short circuit. Therefore their linear usage is limited to adjusting the maximum short circuit current and tuning of switching losses. [16]

2.2.1 Structure

Figure 5 represents the cross section of an n-channel IGBT. It resembles the structure of a MOSFET with an additional p^+–layer on the drain. *P*-channel IGBTs can also be manufactured but this study focuses to the more common *n*-channel IGBTs. The *pn*-junctions are numbered in the figure with arrowed J_X markings. The junction J_2 is the forward-blocking junction during turn-off, and the junction J_1 blocks the reversal voltages. The lower n^+–layer is not essential but it can be used to lower the on-state losses of the IGBT. Also the parasitic thyristor is marked in the figure with a dotted line. [16] Insulating oxide layers between the gate and body region prevents the current flow from the gate.

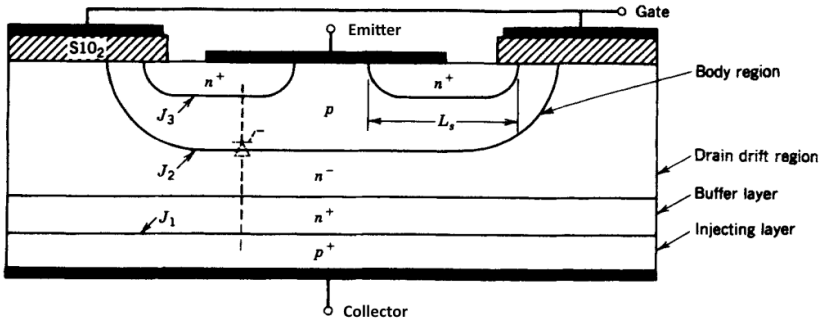

Figure 5. *The vertical cross section of an IGBT. . Adapted from [16].*

Two alternative circuit symbols used for an *n*-channel IGBT is introduced in Figure 6. The first of them highlights the similarity of the IGBT's structure with MOSFET. The second one notes that the structure used for the load current is actually similar to a BJT, but controlled with an insulated gate.

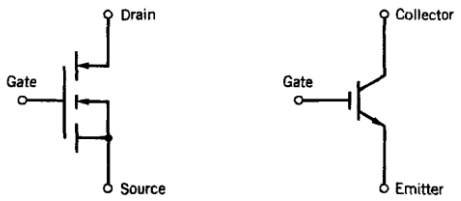

Figure 6. *Two alternative symbols used for IGBT. In this study, the one on the right is used. [16]*

In this study, a variant of the second symbol is mostly used. The reason for this has mainly been the manufacturer of the used IGBT modules, whose datasheets tend to prefer the second option. Note also the alternative naming of power terminals. For clarity, in this thesis the terminals are referred as collector and emitter. The other figures in this thesis are modified to match these expressions.

2.2.2 Controlling the IGBT

N-channel IGBTs are controlled by applying a positive voltage between their gate and emitter. The Figure 7 introduces the transfer characteristics of an IGBT with *the threshold voltage, $V_{GE(th)}$,* marked. The threshold voltage is the virtual border between the on- and the off-state of an IGBT. With gate voltages lower than $V_{GE(th)}$, there is no inversion layer available between the drain and the source. The collector-emitter voltage is applied on junction J_2 and only a small leakage current is flowing through it. [16]

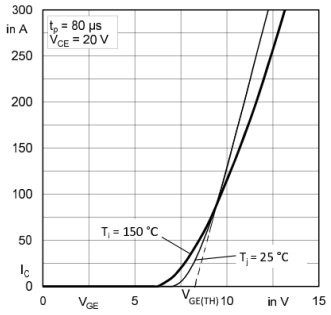

Figure 7. *Typical transfer characteristics of a commercial IGBT module. The threshold voltage marking was added to the figure for illustrating purposes. Adapted from [20].*

When a positive voltage exceeding $V_{GE(th)}$ is applied between gate and emitter, an inversion layer is generated under gate. It creates a conductive path from the n^- on collector drift region to the n^+ region under emitter. The p material on the body region acts as a collector in the structural PNP transistor, while the p+ region on the IGBT's collector is the PNP transistor's emitter and n– drift region is the base. The structural NPN transistor has the n+ region under IGBT's emitter as its emitter, p material as its base and n– drift region as its collector. The structural MOSFET is formed by the same regions as NPN transistor, but having the IGBT's gate as its gate. The structural transistors are marked in the Figure 8 and the equivalent circuit in Figure 9 depicts the functional circuit.

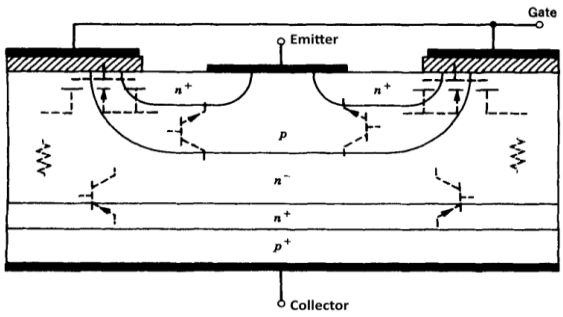

Figure 8. *Structural transistors in the cross section of an IGBT. Adapted from [16].*

Figure 9 introduces the parasitic thyristor in detail, forming of NPN and PNP transistors together with the body region spreading resistance. The body region spreading resistance

is caused by the ohmic resistance of current channel. In Figure 8 it would be located on p-type region under the gate. The thyristor is triggered if the voltage loss over body region spreading resistor exceeds the *pn* junction voltage of NPN transistor's base, allowing current flow from the base to the emitter. That causes the current through NPN transistor's collector and PNP transistor's base to increase, thus increasing the PNP transistor's collector current that forms a continuous voltage loss in body region spreading resistance. The causes of this event are discussed more in Section 2.2.5. [16]

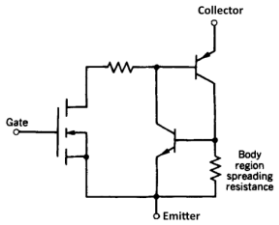

Figure 9. *The equivalent circuit of an IGBT. Adapted from [16].*

To control the IGBT efficiently, the gate voltage has to be forced to a level that is required for IGBT's saturation. The level varies between different models but is normally between 10…20 V_{DC}. Applying a voltage on the gate practically means charging the gate, which represents a non-linear capacitance. Main reason for this non-linearity is the Miller phenomenon discussed later in this section. The required charge depends on the gate voltage swing and the voltage applied over the IGBT. [16] Often the values are not given in the datasheet for more than a couple of operating points. Measuring the gate current, I_G, is the only way to obtain the gate charge value for a certain voltage swing that cannot be found on the datasheet. The gate charge is defined by the integral of the gate current:

$$Q_G = \int I_G dt \qquad (1)$$

The interval of the integration should cover the time from the start of the switching event until the gate current is reduced to zero. [1]

The characteristic output curve of an IGBT is presented in Figure 10. It is visualizes the effects of different gate voltages and collector-emitter voltage to collector current. [16]

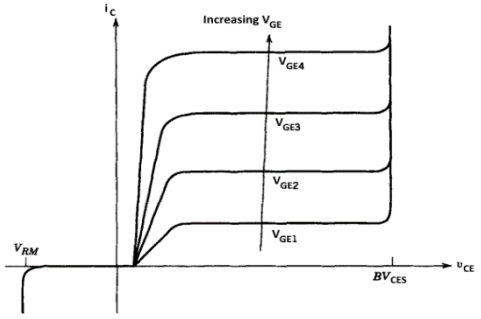

Figure 10. *The characteristic output curve of an IGBT. Adapted from [16].*

During the cutoff state, the current through the IGBT is zero, and the operating point is on the *x*-axis. During on-state, the voltage loss over the IGBT is defined by gate voltage and the load current. Respectively, the maximum collector current allowed for the IGBT can be set by limiting the maximum gate voltage. This information can be used when designing short circuit protections for the IGBT. [16]

2.2.3 Switching characteristics and losses

In this chapter, the main switching characteristics of an IGBT are introduced. As they have many similarities with the characteristics of MOSFETs, some common graphs and circuit diagrams are used. Normally the load driven with a frequency converter is mostly inductive. Therefore the load may be modelled as a constant current source for switching analysis. Equivalent model is introduced in Figure 11. [8] The graphs of Figure 11 describe behavior with an ideal free-wheeling diode, i.e. $v_D = 0$. The switching behavior with a non-ideal diode is described later. The circuit can be considered similar to the frequency converter's main circuit; the switch represents a low-side IGBT, the diode is the free-wheeling diode of a high-side IGBT, and the load is connected from an output phase to DC+ through a conductive high-side IGBT. The low-side IGBT has to be turned off for dead time before the high-side IGBT of the same phase leg can be turned on.

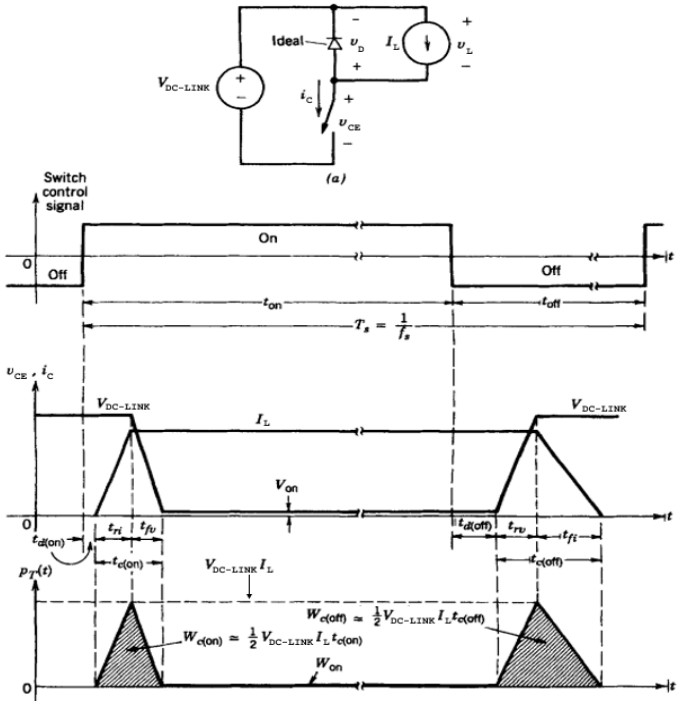

Figure 11. *The equivalent circuit for observing IGBT's switching characteristics and the simplified instantaneous collector current i_C, collector-emitter voltage v_{CE} and power loss p_T including conduction losses W_{on}. Adapted from [16].*

There are different definitions for the switching period. Some sources define the switching to be starting from the change of gate voltage [24], some only take into account the waveforms of collector current and collector-emitter voltage [23]. According to standard IEC 60747-9, the switching period for calculating switching losses starts when the gate voltage has reached a value that is 10 % of its final value and ends when the collector current (turn-off) or collector-emitter voltage (turn-on) has decreased to 2 % level of its original value [23]. However, for this study the limits presented in Table 1 were used.

Table 1. *Limits used for defining the switching period*

Switching event	Starting variable	Value at t_{start}	Ending variable	Value at t_{end}
Turn-on	I_C	10 %	V_{CE}	10 %
Turn-off	V_{CE}	10 %	I_C	10 %

The reason for using threshold conditions other than defined in the standard was the possibility to compare the measurement results to the values given in the datasheet. Using only main circuit waveforms for calculations is advantageous especially when the gate voltage is prone to oscillations [23].

Turn-off switching

According to Kirchhoff's laws, the load current I_L is shared by the diode and the transistor. During transistor's on-state, the load current is dedicated to the transistor and the diode is reverse biased. When the transistor has started to turn off, the current continues conducting through the transistor while the voltage over it increases. The diode stays reverse biased until the v_{CE}, being the transistor's collector-emitter voltage, has reached the level of $V_{DC\text{-}LINK} + v_D$. v_D is the diode's forward voltage during conduction, i.e. $v_D > 0$. When the voltage over the diode reaches v_D, the diode becomes forward biased and current is commutated from the transistor to it. Instantaneous load voltage v_L sets to a slightly negative value, causing v_{CE} to be exceed $V_{DC\text{-}LINK}$. Between the start of turn-off process and the completion of current commutation, both a positive current and voltage are applied over the transistor. That causes the transistor have a power loss during switching as can be noted in Figure 11. [8] The waveforms and equations of losses in the figure are simplified. A precise definition for the losses is defined by the integral over the switching period [24]:

$$E_{SW} = \int_{t_{start}}^{t_{end}} i_C * v_{CE}\, dt \qquad (2)$$

Figure 12 visualizes the switching waveforms in detail. On the waveform of collector current during turn-off, an IGBT-specific phenomenon called *current tailing* can be seen as a decreased slope of the current waveform on period t_{fi2}. First, the MOSFET is able to turn off fast, causing a rapid drop of current during t_{fi1}. After the MOSFET is turned off, the charge remaining on the n^- –region cannot removed by carrier sweep-out. The remaining charges have to be removed by recombination. To gain a low on-state losses, the excess-carrier lifetime and recombination time is designed to be long. [16]

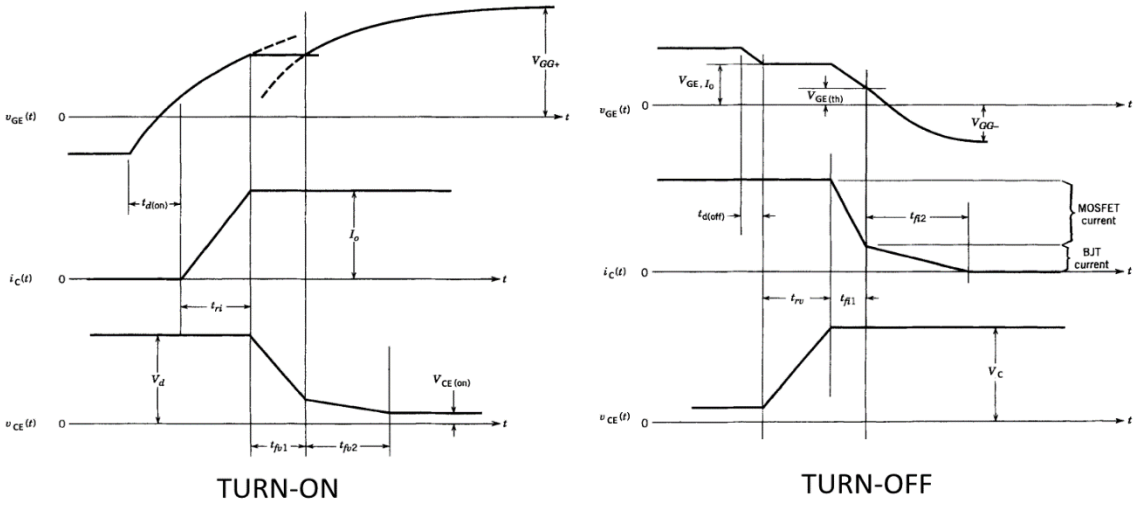

Figure 12. *Switching waveforms of gate voltage (top), collector-emitter voltage (middle), collector current (bottom) of an IGBT. Adapted from [16].*

As the IGBT has to traverse through the linear region when the load current is already conducting on it, the magnitude of the current obviously affects the losses. Figure 13 represents the turn-on and turn-off losses of a commercial IGBT module with the reverse-recovery losses of a free-wheeling diode as a function of IGBT's collector current.

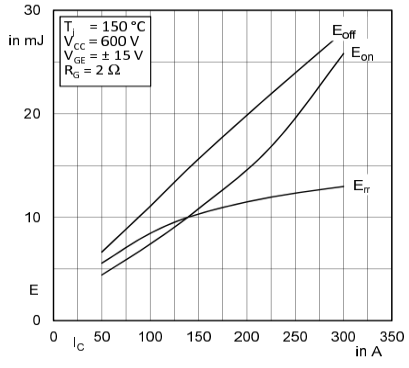

Figure 13. *Typical turn-on and turn-off energies of an IGBT with reverse recovery energy of a free-wheeling diode as function of collector current. [20]*

It can be noted that the current level has almost linear effect on the turn-on energy, E_{ON}, while the turn-off energy, E_{OFF}, seems to have a constant base level of loss. Neglecting that, the dependency between turn-off energy and collector current follows the equation of a straight line. The reason for the constant base level may be caused by current tailing.

Turn-on switching

During turn-on, the diode carries current until the transistor voltage falls below $V_{DC\text{-}LINK}$ and the diode becomes reverse biased. After this, the current commutates to the transistor, whose voltage continues decreasing towards the end value close to zero. Again, the transistor has a power loss during the switching period. [8] The longer the charging and discharging of IGBT's gate takes, the lower will be the slopes of v_{CE} and i_C, and the higher will be the switching losses p_T. As a large part of the losses are caused by switching, it is essential to drive the IGBT's gate with a capable driver circuit. [8]

As for the turn-off switching, also during turn-on the structural bipolar transistor of IGBT changes its state slower than the structural MOSFET. During this time, there is a voltage drop over the IGBT that is higher than the final on-state value. The switching of MOSFET can be observed in the Figure 12 as t_{fv1}, while the switching of bipolar transistor is extended to the interval t_{fv2}. [16] The effect of gate resistor values on the switching losses is later discussed more in Section 2.3.1.

Conduction losses

In addition to the switching losses, there are losses produced during on-state. Since the collector-emitter voltage of an IGBT does not fall to zero during conduction, there is some series resistance that the load current must go through. This can be affected by varying the on-state gate voltage, which is also discussed more in Section 2.3.1.

The total power loss of an IGBT module varies with several factors including the chip temperature, load current, free-wheeling diode characteristics, switching frequency, used gate driver and gate resistors. The temperature affects mainly on the diode characteristics and the on-state resistance of the IGBT chip. [16] The losses are linearly dependent of switching frequency as long as the switching process is completed before the next one.

Miller effect

During turn-on switching, the IGBT's collector-emitter voltage experiences a wide change from the DC-link voltage down to some volts. That affects the voltage applied on parasitic capacitors between collector, emitter and gate, marked in the equivalent circuit in Figure 14.

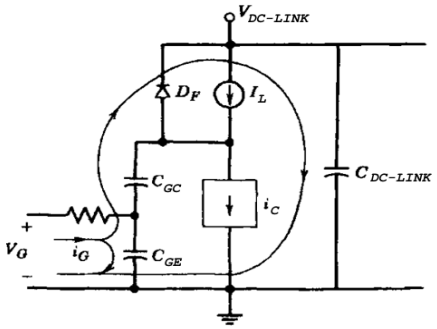

Figure 14. *The equivalent circuit of IGBT's gate driving behavior during turn-on. Adapted from [16].*

The change in voltage causes an increase in the parasitic capacitance between the gate and the collector, C_{GC}, as presented in Figure 15. The capacitance is partly formed by the depletion layer under the gate, which changes its thickness along with the voltage applied over it. The factor for the change can be as high as 10 – 100. [16]

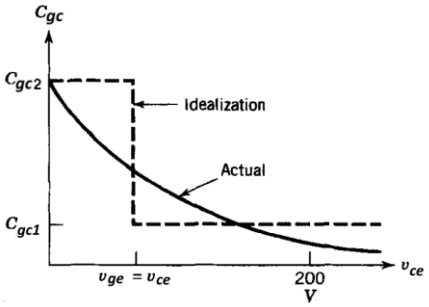

Figure 15. *The effect of V_{CE} variation to the gate-collector capacitance, C_{GC}. Adapted from [16].*

When the IGBT has starting to conduct, the collector current increases until all of the load current has commutated to it. During this interval, the VCE stays constant at a high level and VG increases at a rate defined by the approximated time constant τ_1 ($C_{GC} = C_{GC1}$):

$$\tau = R_{G,ON} * (C_{GE} + C_{GC}) \quad (3)$$

After the collector current has reached its constant value, $I_{C,0}$, the gate voltage gets clamped to a level which is needed to maintain that certain level of collector current. Also the gate current retains its momentary value defined by the gate driver's output voltage, clamped gate voltage and the turn-on resistor [16]:

$$i_G = \frac{V_{DRV} - V_{G,0}}{R_{G,ON}} \quad (4)$$

At that time, all of the gate current is flowing to the Miller capacitance, C_{GC}, causing the IGBT's collector-emitter voltage to start decreasing at a rate [16]:

$$\frac{dv_{CG}}{dt} = \frac{dv_{CE}}{dt} = \frac{i_G}{C_{GC}} = \frac{V_{DRV} - V_{G,0}}{R_{G,ON} * C_{GC}} \quad (5)$$

As already discussed previously, the falling of v_{CE} occurs in two stages. During the first one, t_{fv1}, the MOSFET is turning on and the Miller capacitance C_{GC} remains at a relatively low level, approximated as C_{GC1} in Figure 15. When the MOSFET has turned completely on, the gate voltage starts to increase again with a time constant τ_2, where C_{GC} can now be approximated as C_{GC2}. [16]

For turn-off process, the Miller phenomenon has the same effects. The gate voltage first decreases until the collector-emitter voltage starts to increase rapidly. During the change of v_{CE}, the Miller capacitance is discharged and gate voltage retains its level. After the v_{CE} has reached its final value, the collector current starts decreasing along with the gate voltage. [16]

For driver power calculations, the Miller capacitance can be approximated to be around 400 % in comparison with IGBT's input capacitance, C_{GE}. [4] The input capacitance does not stay constant either, but it only varies on a narrow range due to the smaller variation in gate-emitter voltage. Normally it is approximated to remain constant. [16]

Turn-off voltage overshoot

As the IGBT switches continue developing faster, the requirements for the rest of the main circuit increase, too. Due to the laws of physics, there is always some stray inductance in the main circuit components and connections that store energy in magnetic field. During commutation, the current in the main circuit goes through a rapid change and the amount of stored energy is changed. [6] As the dependence between the rate of change of current, *di/dt*, induced voltage, V_{LS}, and the circuit's stray inductance, L_S, is

$$V_{LS} = L_S * \frac{di}{dt}, \quad (6)$$

a fast decrease in the main circuit current will cause a voltage to induce on the stray inductances of the IGBT module and the rest of the main circuit. [21] This induced voltage will sum up with the DC-link voltage, causing a momentary overvoltage to appear over the IGBT. The higher the di/dt and the stray inductance of the main circuit are, the higher will be the overvoltage. [5] This phenomenon is referred as the *turn-off overshoot.*

Figure 16 represents a simplified equivalent commutation circuit of an inverter phase leg.

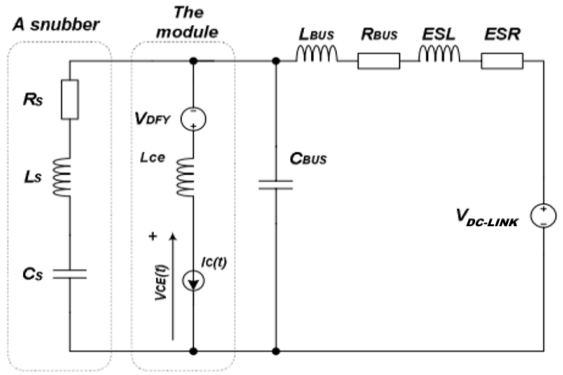

Figure 16. *Simplified equivalent commutation circuit of an inverter phase leg. Adapted from [6].*

The total voltage between the collector and emitter of IGBT can be expressed as:

$$V_{CE} = V_{DC-LINK} + (L_{BUS} + ESL + L_{CE}) \left|\frac{dI_C}{dt}\right| * k_s + V_{DFY} \ , \quad (7)$$

where L_{BUS} is the main circuit bus stray inductance, ESL is the equivalent series inductance of DC-link capacitor, L_{CE} is the stray inductance of the IGBT module, V_{DFY} is the forward recovery voltage of the free-wheeling diode and k_s is a factor taking account the parasitic capacitance of the bus. [6] During switching, the effect of series resistances can be regarded as zero.

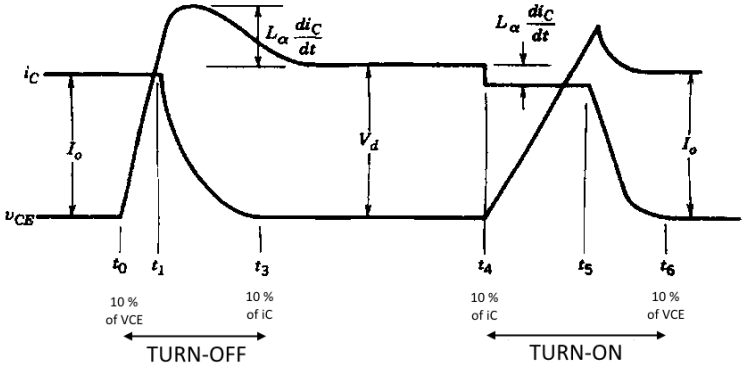

Figure 17. *Principled switching behavior of an IGBT operating in the main circuit of a frequency converter with calculation limits for switching process. Adapted from [16].*

In Figure 17, the principled behavior of an IGBT is presented. Some of the previously mentioned phenomena can be seen in the waveforms of IGBT's collector-emitter voltage, V_{CE}, and IGBT's collector current, I_C. The turn-off voltage overshoot is visible as an increase in the V_{CE} during turn-off. The free-wheeling diode's commutation current peak can be seen in the waveform of i_C during turn-on at time marking t_5. Also the limits of switching process used for calculating losses are marked in the figure. The inductance L_α

represents the total stray inductance on the collector current path. Switching speeds, di/dt and dV/dt, are a trade-off between the efficiency and the caused turn-off voltage overshoots and reverse-recovery current peaks. [6]

2.2.4 Behavior in fault situations

The most common fault situation of an IGBT is driving a short circuit. In power converters, the short circuit impedance can be low, causing high short circuit currents to occur. In this section, two main types of short circuits and the IGBT's behavior in those situations is presented. During short circuit the collector-emitter voltage is significantly higher than during conduction state in normal operation. That takes the IGBT's internal MOSFET to active region, which causes the short circuit current to be dependent of the gate voltage. Higher gate voltage will allow higher current to conduct through the IGBT. If a linearization is made, the steady state short circuit current I_{SC} can be expressed as

$$I_{SC} \approx g_m(V_G - V_{G,TH}) \tag{8}$$

where V_G is gate voltage, $V_{G,TH}$ is gate voltage threshold and g_m is IGBT's transconductance. [6]

Short circuit types

The first type of a short circuit is referred as *hard short circuit.* It has a low impedance and it appears when the IGBT is non-conductive. After turn-on at t_0, the IGBT's collector current increases fast, while the collector-emitter voltage VCE drops to a lower level. V_{CE} shortly returns back close to the DC-link voltage level as can be observed in the Figure 18 between time markings t_2 and t_3. [6]

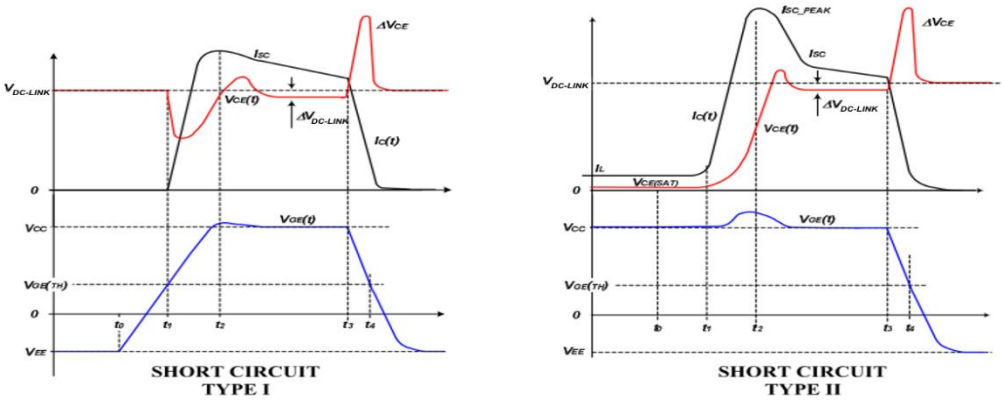

Figure 18. *The characteristic curves of an IGBT during two types of short circuits. Adapted from [6].*

The second short circuit type, *short circuit during conduction,* is caused by appearing of a short circuit when the IGBT is operating in on-state. Before the short circuit appears at

t_0, the collector current is at its normal operational value I_{LOAD} and the collector-emitter voltage V_{CE} is close to zero. After short circuit is formed at t_1, the collector current starts to increase until it has reached the level I_{SC_PEAK}, defined by the transconductance and the gate voltage. This is the maximum level of current that the IGBT can conduct in saturation. As the gate is at higher potential than the collector, the Miller capacitance, C_{GC}, is charged. When the IGBT loses its saturation due to increased current, the V_{CE} starts to increase. The Miller capacitance is discharged through the gate, causing an increase in gate-emitter voltage at time marking t_2, which again causes a large increase in the collector current. [6]

Failure mechanisms of an IGBT

There are three main causes for failure of an IGBT: exceeding the thermal limit of the chip, latching and exceeding the voltage limit. Mainly they are all related to the thermal issues, but the triggering causes can vary [6]. For reasons of safety and delimiting of damages caused my failure, the converter has to have protection against all these three causes. [5]

Exceeding the IGBT's thermal limit is often indirectly caused by a short circuit. A substantial overcurrent will cause excessive heat dissipation in the IGBT chip, leading to a fast increase in the chip temperature. If the *intrinsic temperature* of silicon, being around 250 °C, is exceeded, the control over the IGBT's conductivity will be lost. To prevent this from happening, the short circuit current either has to be limited in some manner, or cut off before the intrinsic temperature is exceeded. [5] Driving the IGBT with high chip temperatures under normal operation reduces the available temperature margin. Often there is an integrated temperature sensor inside the IGBT module that is used for observing the temperature and for controlling the cooling.

Latching (some sources refer to it also as *latchup*) is a state of operation, when the IGBT's structural thyristor is unintentionally turned on. During turn-off process, the IGBT's current is shortly diverted to the IGBT's internal NPN base resistor due to increased body region spreading resistance. If the voltage loss in the body region spreading resistance is high enough, it can cause forward-biasing of the normally non-conductive NPN transistor. After that has happened, the NPN transistor will receive its base current straight from the PNP, resembling the operation of a thyristor. Since thyristors can only be turned off by reducing the current through them to less than holding current, the current flow of a latched output bridge IGBT is not anymore controllable. The DC-link will keep on supplying current to the IGBT until it is destroyed. Latching will eventually cause failure by exceeding the IGBT's thermal limit. Latching can be avoided by reducing the available short circuit current or cutting it before it increases to a harmful level. Lower current

during turn-off will produce a lower voltage loss in the NPN base resistor. [5] As the IGBT's maximum collector current during short circuit can be adjusted by limiting the gate voltage, the same method also helps in preventing latching. Also the switching speed during turn-off affects the occurrence of latching; faster turn-offs will be more likely to cause latching. Often IGBT manufacturers give in their datasheets a maximum allowed peak collector current that can flow without the latching of the IGBT. [16] Latching is mainly caused by short circuit type II [6].

Exceeding the voltage limit represents another failure mechanism. It can be caused by fast turning off of a large current as described in Section 2.2.3, concerning turn-off overshoots. During turn-off, the current rapidly decreases, producing a high di/dt value and therefore inducing an overvoltage that is summed up with the DC-link voltage as can be noticed in Figures 17 and 18. If the voltage over the IGBT exceeds the limit for withstanding, an avalanche breakdown will occur in the semiconductor junctions. During avalanche, the complete collector current is directed to a very narrow current path in the IGBT chip, causing a high current density and local thermal dissipation that leads to losing of current blocking capability [6]. The problem is worst in high current devices and in low operating temperatures. In lower temperature, the recombination in the PN junction is faster [5]. Since the stray inductance cannot be completely removed, the turn-off overshoots are present even in normal switching conditions.

To avoid harmfully high overshoots in a device, whose stray inductances can no more be economically be reduced, the solution is to lower the di/dt either by limiting the short circuit current or by extending the turn-off time. The later can be achieved by either using a higher turn-off resistance in the gate driver or by ramping down the gate voltage. Using a higher turn-off resistance may also enhance the Miller phenomenon and effect the switching losses of the IGBT, and is therefore not an optimal solution. There are also some methods to limit the fault current of the IGBT, such as gate voltage limiting, thus making it possible to use normal overcurrent recognition as protection. [5] Another option would be to react to the overcurrent before it reaches harmful levels, which may be difficult with low-impedance, type I short circuits and would require extremely fast, thus reliable, high current recognition. This study, however, focuses on the solution based on auxiliary soft turn-off circuit triggered by a fast current sensing circuit. This method is further discussed in the Section 2.3.2.

2.3 Gate driver circuits

IGBT gate drivers are a link between the logic control elements and the IGBTs. [6] They are used in converting the low-level signal produced by the controlling logic unit to a proper high-current gate signal. Gate drivers can also house several types of protections and fault recognition circuits, thus delivering information also backwards to the control

system. Lately, also intelligent drivers with integrated logical processor have been introduced. [4] This study considers only non-resonant gate drivers. Resonant gate drivers are used mainly on applications with higher switching frequencies. [1]

The output stage of a conventional IGBT gate driver consists of two output current channels: one for turning the IGBT on, and another for turning it off. The simplified circuits are presented in Figure 19. The channels are simple circuits supplied by a single or dual voltage supply that is tied to the emitter of the driven IGBT, a low-impedance semiconductor switch and a gate resistor. The gate resistors limit the gate current and the switching speed of the IGBT. [6] The driver's supply in further chapters is regarded to be a dual voltage supply, capable of offering also negative voltage for the driver.

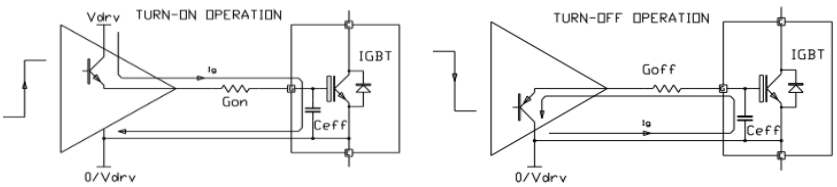

Figure 19. *The principled gate current paths during switching. [4]*

Basically the IGBT's gate is wanted to be connected to either driver's positive or negative supply voltage. Floating gate could lead to unintended switching. When considering an ideal gate driver, the supply voltage levels have the dominant effect on the IGBT's switching behavior along with the values of gate resistors. An ideal gate driver is capable of providing infinite gate current with zero delay, making it possible to adjust the gate voltage slope solely by defining suitable values for gate resistors and driver supplies. The operation real driver circuits, however, is limited by the same phenomena that has been introduced in the previous sections: stray inductance and capacitance, series resistance and the non-ideal switching characteristics of transistors. In this section, the design constraints and characteristics of gate drivers are discussed in detail together with, considering this study, the most significant additional driver features.

2.3.1 Requirements for a gate driver

To be capable for driving the IGBT efficiently and reliably, the gate driver circuit has to fill several requirements in terms of delays, maximum output current, heat dissipation, thermal stability, variability of component values caused by tolerances, interference and voltage stresses especially on the isolated high-side drivers. This chapter will go through a short presentation for the theory and design constraints regarding them.

Power demand

The driver circuit has to be able to handle high enough power to charge and discharge the gate during continuous operation. The theoretical minimum power demand for the driver is the power needed for changing the state of the IGBT's gate:

$$P_{DRV} = Q_G * f_{SW} * \Delta V_G + C_{G,AUX} * f_{SW} * \Delta V_G{}^2 , \quad (9)$$

where P_{DRV} is the driving power that is delivered to the gate, Q_G is the gate charge for the given gate voltage swing ΔV_G, f_{SW} is the switching frequency and $C_{G,AUX}$ is the capacitance of auxiliary gate capacitor. [1] It has to be noted that a certain value of Q_G is valid only at one operating point and depends not only on high and low values of gate voltage, but also on the IGBT's collector-emitter voltage due to changing Miller capacitance, C_{GC}. The formula only gives the power needed for driving the gate. In addition to that power, all the losses of the driver have to be taken into account.

The charge of the auxiliary gate capacitor can be calculated with formula (10):

$$Q_{G,AUX} = C_{G,AUX} * \Delta V_G , \quad (10)$$

where $Q_{G,AUX}$ is the charge of auxiliary gate capacitor when it is charged to the same final voltage as the gate. [21] The formula simplifies the calculation by assuming that the gate will always reach its final voltage during pulse. In most applications the assumption is justified due to relatively short time constant of gate resistors and gate equivalent capacitance. [1] Therefore the total charge $Q_{G,TOT}$ that must be delivered to the gate every switching cycle is the sum of equivalent gate charge Q_G and the charge of auxiliary gate capacitor, $Q_{G,AUX}$.

Output impedance and gate resistors

The second essential quality for a gate driver is the current supplying capability and low output impedance related to it. Available gate current level affects the time that the IGBT stays on linear region during switching and therefore to the main circuit switching losses. Since the auxiliary gate capacitor represents a short circuit immediately after switching, it is required that the driver can provide at least a maximum current $I_{DRV,MAX}$:

$$I_{DRV,MAX} = \frac{\Delta V_G}{R_{G,MIN}} \quad (11)$$

where ΔV_G is the gate voltage swing and $R_{G,MIN}$ is the minimum allowed gate resistor value. Typically the stray inductance of the gate driving traces and wiring reduce the real

maximum gate current to only 70 % of the calculated maximum current, when low-resistance gate resistors are used. [1]

If the output transistors switch fast and are able to provide sufficient gate currents, adjusting the IGBT's switching times can be done by selecting appropriate values for gate resistors. This makes the driver usable for various applications where different IGBTs are present. As mentioned previously, choosing gate resistor values is making a compromise between switching losses and allowed transient levels. Even though high switching speeds produce lower switching losses, there are some factors that limit the lowest usable gate resistor value. Using too low turn-on resistor value may cause exceeding EMI restrictions, oscillation in the IGBT's collector current or reversal high current peaks through the free-wheeling diode, depending on the recovery time of the diode [4] [22]. Too high transient values can even cause failures in the load motor windings.

Figure 20 presents the turn-on and turn-off energies of an IGBT and the reverse-recovery energy as a function of gate resistor values for a commercial IGBT module. The first issue to note is the strong dependence between turn-on energy, E_{ON}, and gate resistor value. The second issue is that effect is only marginal when it comes to turn-off energy, E_{OFF}. The difference between the relationships of these two energies can be explained by the non-linearity of IGBT's operation. The linear region, where most of the losses are caused, is located on the upper part of the gate swing range, beginning from around 7 V according to Figure 7, found in Section 2.2.2 and representing the same IGBT module.

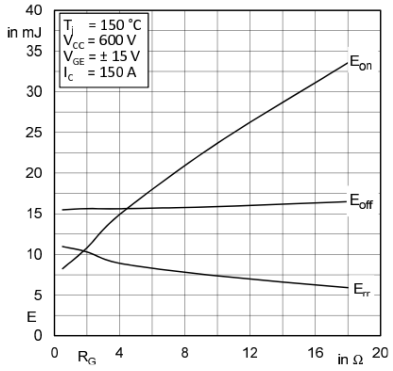

Figure 20. *Typical turn-on and turn-off energies of an IGBT together with reverse recovery energy of a free-wheeling diode as a function of gate resistor value. [20]*

As the gate is charged with a positive voltage supply through the turn-on gate resistor, the slope of the curve decreases along with the increasing voltage. Therefore charging of the last volts to the gate takes a significant time, which is yet extended due to the Miller effect. During turn-off, the linear region is located in the beginning of the discharging curve, when the discharging current is still at a high level. This allows the gate voltage to fall rapidly, thus reducing the losses caused by operating on the linear region.

As a final note of the figure, it can be seen that the reverse-recovery energy is slightly decreasing when the gate resistor value is increased. Slower switching causes the current to commutate slower from the diode to the IGBT during turn-on. This ensures longer time for the diode to change state, thus reducing the reversal current peak and energy loss.

Noise immunity

The operational environment close to the switching elements of the main circuit exposes the gate driver to harsh electromagnetic noise. The location as close to the IGBT as possible is needed to minimize the inductance on the gate current path. The high values of di/dt and dV/dt in the main circuit cause interference that the driver circuit should be able to take without letting it to affect the operation. [3]

One important factor in reducing the gate inductance is using the so called *Kelvin emitter* which is an additional pin connected to the emitter of the IGBT chip. It lowers the stray inductance of the bond wires but also reduces the negative feedback that is caused by the voltage loss in the bond wires on the main circuit current path. [4] The effects of Kelvin emitter to the IGBT's switching characteristics are further discussed in Appendix C. Additionally, it should also be taken care that if the isolation of high-side drivers is done optically, the input signal for the optocoupler should be properly filtered to avoid false driving commands. [14] The same applies for the driver circuit, if low voltage logic or measurements are included.

Output stage transistors

The output stage of the gate driver forms an amplifier that is used to drive the gate through the gate resistors. Depending on the structure, the input signal for the output stage can be either voltage or current signal. This study focuses on a BJT-based output stage and therefore also the controlling signal form is current [21]. The output of the amplifier, or *push-pull stage,* can be regarded as voltage signal, whereas the gate resistors are used to limit the gate current. In this study, the output of the driver circuit is measured between the output stage transistors and gate resistors. This is done to verify the actual potential of the driver in terms of voltage change rate under load rather than measuring its operation at one gate resistor value. By using low-impedance load in the output during measurements, it could be assured that the driver's output stage transistors operate as intended, i.e. without limiting the gate current by drifting from quasi-saturation into linear region.

Using MOSFETs instead of BJTs in the driver's push-pull stage would have some advantages in terms of controllability and delays. MOSFETs are in general easier to control than BJTs, because they are controlled by gate-source voltage rather than a continuous

base current. Like IGBTs, MOSFETs designed for large currents tend to have a large parasitic input capacitance which has to be charged and discharged during each switching event. That makes the controlling more complex, since fast switching requires large gate currents. [21] On the other hand, BJTs are current-controlled devices, which may give them an advantage in the means of robustness and good noise immunity. The BJTs need a continuous base current for maintaining the conductivity in the switched circuit. The minimum required base current, I_B, is:

$$I_B = \frac{I_C}{\beta}, \tag{12}$$

where I_C is the collector current and β is the transistor-specific gain. For high-current BJTs required for gate drivers, the gain is normally lower than for the BJTs designed for signaling. This causes additional power loss in the driver circuit, which may lead to a notable decrease in efficiency in low power converters. [8]

The turn-on time of a BJT depends on the delivery time of the stored charge to the base. The delays of the gate driver's output stage will cause the main circuit switching times to extend and losses to increase. The delays can be compensated by implementing an additional circuit that delivers a high-amplitude current pulse to or from the base during switching instead of constant current. The *boosting circuit*, introduced in Figure 21, can be as simple as a parallel RC circuit that is connected in series with the controlling signal. [8] The high-amplitude base current pulse will provide or remove the stored charge for the junction, momentarily drive the transistor closer to the saturation and therefore speed up the beginning of the switching process. After switching, the capacitor does not affect the operation and the base current is constant.

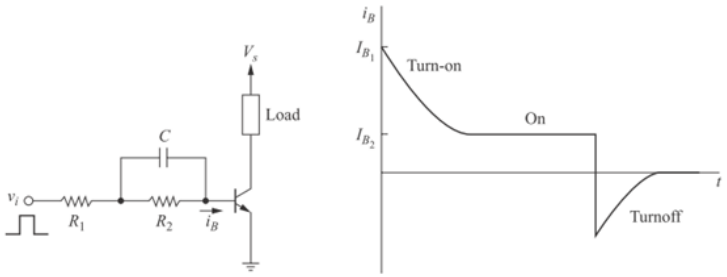

Figure 21. *A simple RC circuit can be used to boost the base current during switching. [8]*

Another characteristic for BJTs' switching is the extending recovery time when the transistor is let to enter hard saturation. For reduced switching times, it is beneficial to keep the transistor in so-called *quasi-saturation region*. In quasi-saturation, the transistor operates between linear and hard saturation regions. [8] In hard saturation, the collector-emitter voltage is low, and a higher share of the charge carriers passing collector is delivered to the base instead of being swept to the emitter. [21] If the decrease of V_{CE} during

conduction state is limited to an appropriate value by reducing the base current, the transistor will recover fast. As a downside for this, there will always be a voltage loss of ~1 V over the BJT, producing higher power loss than a saturated BJT would. [8] Also the needed power supply voltages have to be higher to achieve the same output voltage. One solution for driving the transistors in quasi-saturation region is introduced in Figure 22. The circuit, referred later as *desaturation circuit*, is also known as a *Baker's clamp.*

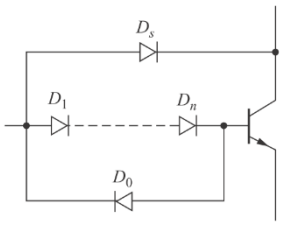

Figure 22. *Baker's clamp acts as a circuit that prevents the BJT from entering saturation. [8]*

The number of diodes in series with the base define the on-state collector-emitter voltage V_{CE}. When the V_{CE} starts to sink, current from the controlling source is redirected straight to the collector instead of base. Since the control current is usually limited, this causes a reduction in the base current. The circuit finds a balance, where the collector voltage is around $(n - 1)*V_D$ above the base, V_D being the forward voltage of a diode. D_0 can be added to offer a current path for reverse base current during turn-off. [8]

Switching frequency in medium power frequency converters is normally in the range of 2…16 kHz. The frequency can be regarded fairly low for gate driver circuits and is therefore not a limiting factor. The switching frequency, however, should be taken into account when calculating the power consumption and thermal capability of the driver. Higher switching frequency will cause the driver's power consumption to increase mainly by increasing the heating of gate resistors and transistors. [1]

High-side driver isolation

Since the IGBTs are controlled by gate-emitter voltage, the gate drivers have to be able to provide a voltage output that is always referenced to the IGBT's emitter. As visualized previously in Figure 4, for low-side drivers, this means a connection from the driver to the DC– while the high-side drivers have to be connected to the output phase. In principle, this means that the high-side drivers have to be floating in respect with the DC-link. During normal operation, their reference potential is switched between ([DC+] – $V_{CE,ON}$) and DC– with the output phase. [16]

The isolation is normally done either by optocouplers, fiber optics or transformers. The optocoupler introduced in Figure 23 consists of a LED, a phototransistor and a Schmitt

trigger circuit that reduces oscillation during switching. Between the LED and the transistor there is a transparent gap that creates the isolation between the input and output. The basic problem of optocouplers is the parasitic capacitance over the gap, causing the LED to light up unintentionally if the common mode voltage transient over the gap is high enough. This is usually reduced by adding a shield layer to the gap. Fiber optics share the same basic structure but the light is delivered by an optic cable, which eliminates the problem of false triggering due to increased gap length. The transmitter and receiver can be located on different boards. [16] The optocouplers also tend to have a significant propagation delay. [24]

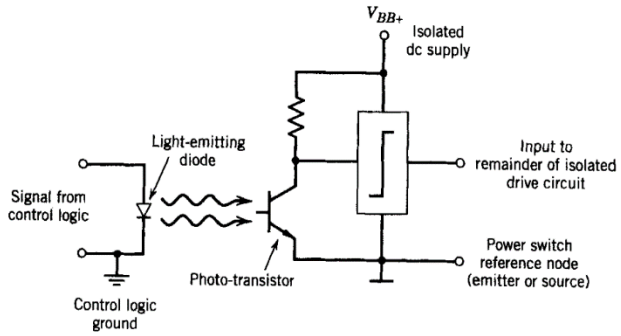

Figure 23. *The principled schematic of an optocoupler. [16]*

Using transformers and magnetic instead of optical isolation is another option. Although small, high-frequency signal transformers tend to have a lower capacitance between input and output than optocouplers, they are not as commonly used in frequency converters. Example circuit of a control signal modulated high-frequency isolator can be found in Figure 24. Since the switching frequency of frequency converters is relatively low for magnetic coupling, higher carrier frequency can be used to reduce the size of the transformer. One advantage of using transformer isolation would be the possibility to combine power supply and signal isolation to one transformer. [16]

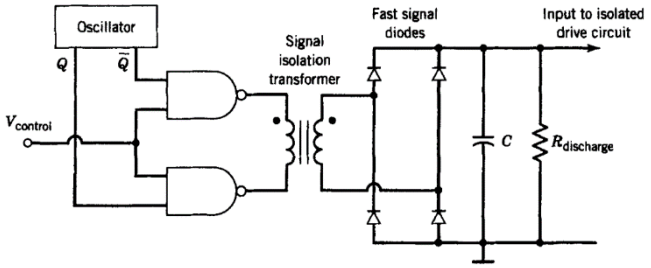

Figure 24. *The schematic of a control signal modulated magnetic isolator. [16]*

By using isolation on the low-side drivers, the delays can be set equal with high-side drivers and managing the dead times becomes easier. It also helps to minimize current loops in DC- net and to delimit the coupling of interference from the main circuit to the control circuits.

Sufficient steady state voltages for IGBT's gate

As discussed previously in Section 2.2.3, the effect of the final steady-state levels of gate voltage is significant. Figure 25 introduces the conduction state characteristics of a commercial IGBT module. The curves in the figure represent typical saturation voltage levels of V_{CE} as a function of collector current and different gate voltages [20].

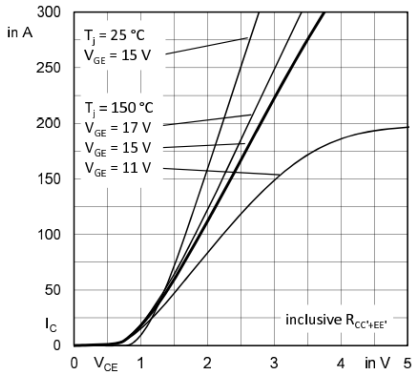

Figure 25. *The dependence between collector current and collector-emitter voltage of an IGBT with different values of gate-emitter voltage and junction temperature. [20]*

According to the datasheet of the IGBT module selected for the driver investigations, the nominal collector current of the module is 150 A. Depending on the gate voltage, the V_{CE} can vary between 2,2…3,1 V, meaning a 41 % increase in conduction losses if the gate voltage is lowered from 17 V down to 11 V.

As discussed earlier in Section 2.2.3, the turn-on switching speed is more prone to cause losses than the turn-off. As the final on-state voltage of the gate is dependent of the driver's positive supply voltage, lowering it would slow the switching speed and increase the switching losses. The effect of negative supply voltage is not that visible, since the linear region will still be passed fast and the gate stays negative ensuring that the IGBT is non-conductive during off-state. It is also essential that the driver's output voltage is not prone to oscillation as it may cause additional losses in the main circuit [1].

Delay, jitter and dead time

As already mentioned in Section 2.1.1, simultaneous conduction of both high- and low-side IGBTs of the same output phase leg, referred as *a bridge shoot through* or *a short cross conduction*, has to be avoided. When occurring, the shoot throughs cause a short circuit between DC+ and DC–, which again leads to increased losses in the main circuit or even thermal runaway of the IGBTs. The prevention is done by implementing a dead time which is a time interval without any driving signal to the IGBTs. [24]

There are two types of dead times, called as *control dead time* and *effective dead time.* Control dead time is implemented in the control system, causing a gap between generating driving signals in the signal processor. Effective dead time is the time the IGBTs actually are non-conductive simultaneously. Control dead time is set to provide a positive effective dead time under worst case conditions, taking into account variation in component tolerances, thermal drifting of setting values as well as asymmetrical, current- and temperature-dependent switching characteristics of IGBT, etc. In optimal situation, the effective dead time would be close to zero. However, due to designing for worst case situation, under normal operating conditions the effective dead time will usually be significant when compared to the control dead time. [24]

As a downside effect, the output voltage of the converter during dead time is defined by the direction of output current rather than control signals. When driving an induction motor, it may also cause instability of the converter and damage for the motor. Therefore it should be set to the minimum level that satisfies the requirements for safe operation. [24] Since the control dead time is set by the logic processor, it is sufficient for this study to understand the need for it and the factors in the driver circuit that affects its value, i.e. the driver's delays and thermal behavior.

Often the main sources of delay of the driver are the optocouplers and gate resistors. Since the IGBT's gate capacitance forms a low-pass filter together with the gate resistors, using higher gate resistor value will cause an increase in the switching delay. The gate resistor causes delay not only to the IGBTs traverse on the linear region, but also to the time between the turning of the driver's output and the change in the gate voltage. [24] Additional delay will be caused by the non-ideal operation of other circuitry, such as finite rise and fall times of level setting circuits. The driver's output stage transistors are also prone to cause delay, as especially high current BJTs have a long turn-off time when compared to their turn-on time. As discussed earlier in this section, the behavior is highlighted when the transistors are driven close to saturation [8].

There are some main sources of variability in the driver's delay. The variation between transfer times of signals can be referred as *jitter*. Jitter can be caused by, for example, crosstalk from radiated or conducted signals, dispersion effects or impedance mismatch. [7] Additionally, propagation delays of optocouplers and driver ICs vary [24]. The total delay of the driver circuit with jitter variance has to be taken into account when designing measurements, protections and controlling elements that operate on the switching frequency. Neglecting delays will cause false or missing alert signals. This is highlighted especially when driving parallel IGBT modules with individual gate drivers.

2.3.2 Additional features of a gate driver

In this chapter, some enhancements and protections for the gate driver circuit are presented and the theory behind them introduced. When implementing protections to the driver circuit, it has to be made sure that the highly noisy environment does not cause false alarms or unintentionally affect the normal operation of the gate driver. The protections should also be able to operate under situations of when a short circuit is generated during conduction, but also when the short circuit is already present in the beginning of the switching process. [5]

Auxiliary gate capacitor

To minimize IGBT's switching losses, it is beneficial to set the rates of change for collector current and collector-emitter voltage, di_C/dt and dV_{CE}/dt individually. The goal is to set the turn-on resistor $R_{G,ON}$ to the minimum level defined by the reverse-recovery time of the free-wheeling diode and then maximizing the value of dV_{CE}/dt. As known from Section 2.2.3, the collector current has already reached the final value before the collector-emitter voltage even starts to change. [22]

During turn-on the di_C/dt is set by the time constant of RC circuit formed by gate resistor together with the parallel connected auxiliary gate capacitor and gate-emitter capacitance, C_{GE}. Therefore the di_C/dt can be decreased by increasing the capacitance on the gate, i.e. auxiliary gate capacitor. During turn-off, the auxiliary gate capacitor increases the switching time. That often causes a need for using a lower value for turn-off gate resistor, $R_{G,OFF}$. [22]

For V_{CE}, the traverse takes place together with the charging or discharging the Miller capacitance, C_{GC}. Since the C_{GC} is charged/discharged through the gate resistor, the dV_{CE}/dt can be adjusted by its resistance. [22] This use of auxiliary gate capacitor is valid mainly for the IGBT modules without internal gate resistors. With the modules including an internal gate resistor, its resistance often dominates the used external gate resistors.

It may also be advantageous to use an additional damping resistor in series with the auxiliary gate capacitor to avoid oscillation between the gate capacitances and the stray inductances on the gate path. Internal gate resistors will help to avoid oscillation. [22] On the other hand, the auxiliary gate capacitor reduces oscillation of the driver circuit during output phase short circuit situations. It should be designed to be around 10 % of the equivalent gate capacitance with the used on-state gate voltage. [3]

Soft turn-off function

Soft turn-off is a generic term for a slowed turn-off switching event. Although there are several ways to implement this functionality to the gate driver circuit, the main idea of operation is shared. In normal switching events, the current to and from the IGBT's gate is limited by the turn-on and turn-off resistors. They are designed to yield a relatively fast switching, which decreases the losses of IGBT and the needed dead time. Under short circuit condition, the IGBT's collector current increases significantly faster than under normal operation, and therefore may have already exceeded the safe operation limits when the short circuit is detected and the drive reacts to it. In such case, the normal turn-off would be too fast and cause harmful overshoot voltages to appear over the IGBT.

Soft turn-off is used to slow down the turn-off switching process by offering higher resistance on the current path used for discharging the gate's parasitic capacitances and the auxiliary gate capacitor. Since the resistance is higher, the gate current is lower and the discharge time longer than in normal turn-off. Since the IGBT is a voltage-controlled device, the slowly decreasing gate voltage affects also the duration of IGBT being on its linear, lossy region. While the turn-off process takes more time, the change of the collector current during turn-off, di_C/dt, is lower. Further, this affects the amplitude of overvoltage induced in the stray inductances of main circuit. [6] Soft turn-off can be used for all kinds of fault shutdowns, but it is advantageous only if a high current is conducting through the IGBTs.

Since the soft turn-off is activated only during a fault situation, simultaneous normal modulation is inhibited. Therefore the soft turn-off pulse can be longer than the normal driving pulses without causing overlapping of driving signals and short cross conduction. However, as mentioned previously, using a higher resistance in gate discharging affects the duration of the turn-off. Even if the overshoot is lower, too high resistance can cause excessive local heat dissipation in the IGBT chip, which can lead to a damage. It will also cause delay to the start of turn-off, letting the short circuit current continue increasing even if the short circuit is already detected. [6]

Since the IGBT operates in its linear region during short circuit, the short circuit current can be controlled by the gate voltage. Formula 13 introduces the dependence between the resistance used for discharging the gate, $R_{G,OFF}$, and collector current slope, dI_C/dt:

$$\frac{dI_C}{dt} = \frac{V_{EE} - V_{GE(TH)} - \frac{I_{SC}}{g_m}}{\frac{R_{G,OFF} * C_{GE,TOT}}{g_m} + L_E} \approx \frac{V_{EE} - V_{CC}}{\frac{R_{G,OFF} * C_{GE,TOT}}{g_m} + L_E}, \tag{13}$$

where V_{EE} is the negative and V_{CC} the positive gate supply voltage, I_{SC} the short circuit current, g_m the trans-conductance of the IGBT, L_E the Kelvin emitter contact stray inductance, $V_{GE(TH)}$ is the gate threshold voltage and $C_{GE,TOT}$ the total gate-emitter capacitance at used gate voltage swing, taking into account the capacitance of auxiliary gate capacitor. L_E acts as a negative feedback in the circuit. As the formula depicts, the slope can be reduced either by increasing $R_{G,OFF}$ or $C_{GE,TOT}$, or by decreasing the IGBT's trans-conductance. The turn-off resistance is the only one that can be easily varied. [6] Final value of the resistance should be defined after measuring the overvoltage and the caused additional delay.

Short circuit recognition by V_{CE} measurement

One possible method to detect short circuits in the output of the converter is to monitor the collector-emitter voltage of an IGBT, V_{CE}. During turn-on switching the V_{CE} should change its state from the value of the DC-link voltage to some volts in a couple of microseconds. Under short circuit conduction the magnitude of IGBT's collector current becomes significantly high, which prevents the IGBT from entering saturation as discussed in Section 2.2.4. This causes the V_{CE} to set to a voltage that is more than the common on-state voltage but less than the DC-link voltage. By observing the V_{CE} for such situations, the short circuits can be detected in a relatively short time without using the ordinary current measurement. [19] Yet another possibility for fast short circuit recognition is to monitor the voltage loss on the IGBT module's emitter bond wiring [17] [18].

The main problem with the short circuit detection based on the V_{CE} measurement is that the sweep of VCE from the voltage value of DC-link to almost zero during switching events has to be distinguished from the short circuits in some way to prevent false alarms. Usually this is achieved by ignoring the fault signals for a certain amount of time after switching. The delay is referred as *detection blanking time* [4]. In low-inductance and low-resistance short circuits, the current may already in that time interval increase to a level, which could cause damage if the corresponding IGBT if an ordinary turn-off routine is applied. [6]

It can also happen that both the high- and low-side IGBTs are turned on simultaneously due to erroneous signals, interference, gate driver failure or too short dead times. Such situations are referred as *short cross conduction.* If the problem is caused by overlapping of high- and low-side conduction periods, the short circuit may disappear before the detection blanking time is over and therefore be left unnoticed. That may cause additional losses to the IGBT chips even if they are not instantly damaged. [4] In the studied design, this kind of short circuit recognition was not added on the prototype but the interface was built to support an external short circuit monitoring signal.

3. DRIVER PROTOTYPE AND MEASUREMENTS

This section focuses on the developed driver circuit and the research methods that were used for verifying the operation. Although there are a vast number of existing driver circuits based on various topologies, the driver most of the times needs to be adjusted for each application [4]. This decreases the usability of some existing solutions that are designed for older, slowly switching IGBTs. Some academic researches and their outcomes focus on the technical structure, while the commercial point of view is not taken into account. This may cause the driver to be suitable for only some special application [17] [19]. In commercial design scene, easily scalable solutions are desired [4]. There are also some verified driver circuits available in the company's design database, but they all have their weaknesses. Some may not be able to provide high gate currents, some may require two separate dual supplies for the driver stage and some are higher at cost. The soft turn-off was also available for only one driver, but it was designed for lower gate currents.

Numerous articles and technical solutions for the soft turn-off functionality are available in the academic databases and manufacturer's publications, but they have not been widely implemented in the company's converters [5] [6] [19]. Many of them also focus on local short circuit recognitions and protections constructed on the driver circuit, which was not desired for this scope [5] [6] [17] [19]. The studied soft turn-off circuitry is simple and adds only a few additional components to the driver circuit, which offers a vantage over the company's previously used circuits. Simple design eases the adjusting, thus making the implementation of the circuit to new products faster.

The development of a new driver was started to combine the advantages of the existing driver circuits and to develop an effective method to reduce turn-off overshoots under short circuit conditions. The development of the driver is the first part of a research whose goal is to develop a short circuit proof IGBT driver system. After finishing the driver, the research will continue by developing the fast di/dt recognition circuitry that would trigger the soft turn-off function. If proven usable, the driver system may be considered as option for high power, premium class converters.

During the design phase, several tools were used including PSpice 16.1 for simulations, PADS 9.5 for designing schematics and layout, Altera Quartus 14.0 for constructing the control logic, and CAM350 for reviewing the produced PCB manufacturing images.

First, the block diagram of the prototype is introduced, followed by presentation of schematics and simulation results. Most of the images are added in appendixes due to their size, including schematics of both PSpice and PADS with layout and assembly images. Simulation results are not presented, since most of the data gained was fairly well in line

with the measurement results. Additionally, the reference circuit used for appraising the qualities of the prototype are introduced. Finally, the methods and equipment used for verification are discussed. This includes the justification for data processing and the means for measuring the operation of the circuit.

3.1 Built prototype and its basic functions

The reason for starting this study was to reveal the usability of the drafted driver circuit and to find out if the turn-off overshoots with high load currents could be handled with soft turn-offs. To gain this information, simulations of the driver circuit were run, a prototype PCB was drawn, manufactured, tested and adjusted, and finally the complete test system was used for measurements. The prototype was needed for fine-tuning the component values, since the simulator component models are known to be occasionally simplified or idealistic. Also the driver's behavior with a high voltage DC-link and the effects of main circuit stray characteristics would have been difficult to simulate.

The prototype was mainly used for three purposes:

- Adjusting and testing the operation of the driver circuit
- Testing the Gate Soft Turn-off function and solving the dependencies between the turn-off overshoot voltage amplitude V_{TO} and the values of soft turn-off resistor R_{GST} and capacitor C_{GST}
- Testing the IGBT module characteristics

Since the IGBT module was already measured with another driver, it was not needed to study its behavior in detail. The module was, however, measured at some operating points in order to clarify, how the driver affects the main circuit performance. Additionally, the prototype will be used for developing the di_C/dt detection circuit and combining the alert signal to the soft turn-off function.

The developed prototype was named as *70CVB01979A Gate Soft Turn-off Proto Board* according to the company's naming practice and consists of functions listed in block diagram of Figure 26. The main purpose of the prototype is to provide an user interface for creating desired test pulses for studying the IGBT module's and the driver's behavior at different operating points. The prototyping board consists of two parts that can be physically separated for safe testing in laboratory environment. The main part of the board simulates the power board of a frequency converter, while the detachable part acts as a combined measurement and I/O board. Later this detached part of 70CVB01979A will be known as *control board.*

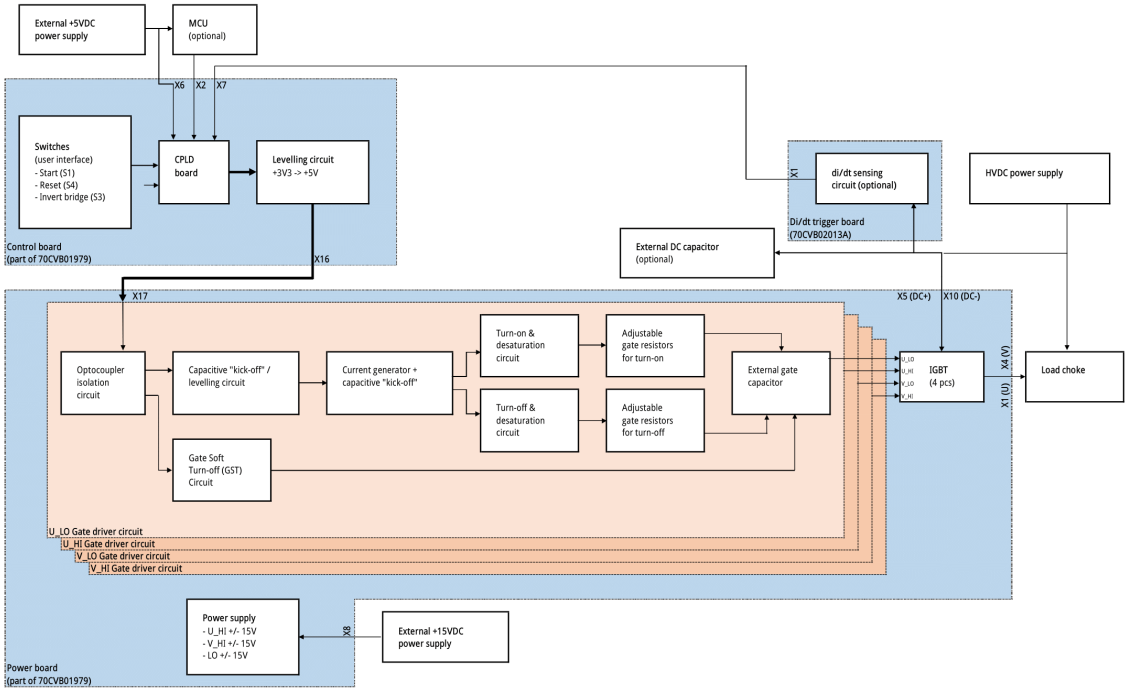

Figure 26. *The functional block diagram of the developed driver circuit with additional equipment used in the test setup.*

The control board provides the user interface, connection for the programmable logic development board, signal levelling/conversion circuit and the connector for the gate driving signals delivered to the power board. The control board, presented in Figure 27, needs an external power supply of +5 VDC. All the nets on the control board are isolated from the high voltage side by optocouplers, located on the power board. For safety reasons, the functional isolation in the laboratory was done by using an extension cable between the control and power boards, and adding an insulating plastic plate between the user interface and the high voltage parts.

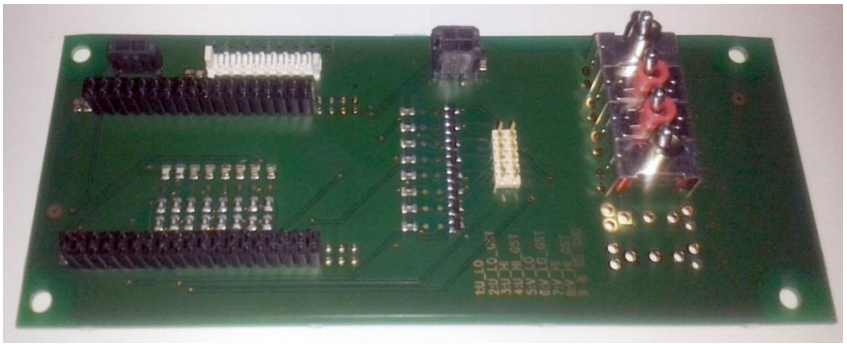

Figure 27. *The control board with four assembled switches (S1-S4) on the right, the CPLD evaluation board interface (X2-X3) on the left, the +5 VDC power supply input connector (X6) on the top-left corner and the gate signal output connector (X16) on its right side.*

The user interface consists of switches that are connected to the programmable *CPLD (Complex Programmable Logic Device)* development board, providing the required precision timing for the pulse generation. The CPLD board is attached to the control board with a pair of two-row pin headers. The CPLD board outputs low-level voltage signals that are converted on the control board to current signals and delivered to the power board through a ribbon cable. The number and the length of the gate pulses can be set by the user with a PC software (Altera Quartus 14.0) and a programming tool (Altera USB Blaster II). The CPLD board was chosen as the logic unit for the prototype due to its sufficient 50 MHz clock and possibility to execute several functions simultaneously. There was also a basic frame for the logic description available from previous prototypes.

The power board, presented in Figure 28, consists of four gate driving circuits, one for each IGBT switch. For each gate driving signal, there is an optocoupler that provides electrical isolation between user interface and the high voltage side, a push-pull type driver, adjustable gate resistors and an external gate capacitor. In addition to that, in parallel to each driver there is a circuit that can carry out a so called *Gate Soft Turn-off (GST)* function. GST function is used to bypass normal gate driving signals and slowly discharge the gate capacitance in case of output phase short circuit, leading to a slow turning off of the IGBT's current. This is desired due to high recovery voltages during fast turn-offs that can lead to breaking of IGBTs. On the prototype, the GST function can either be operated by setting a time delay or by using an external di/dt triggering circuit. The test setup was designed to use another prototyping board as an over-current trigger source, as can be seen in the block diagram of Figure 26. The driver can be used with or without GST functionality and di/dt trigger source. The di/dt circuit and its interface have been left out of the scope of this study and therefore not introduced in detail.

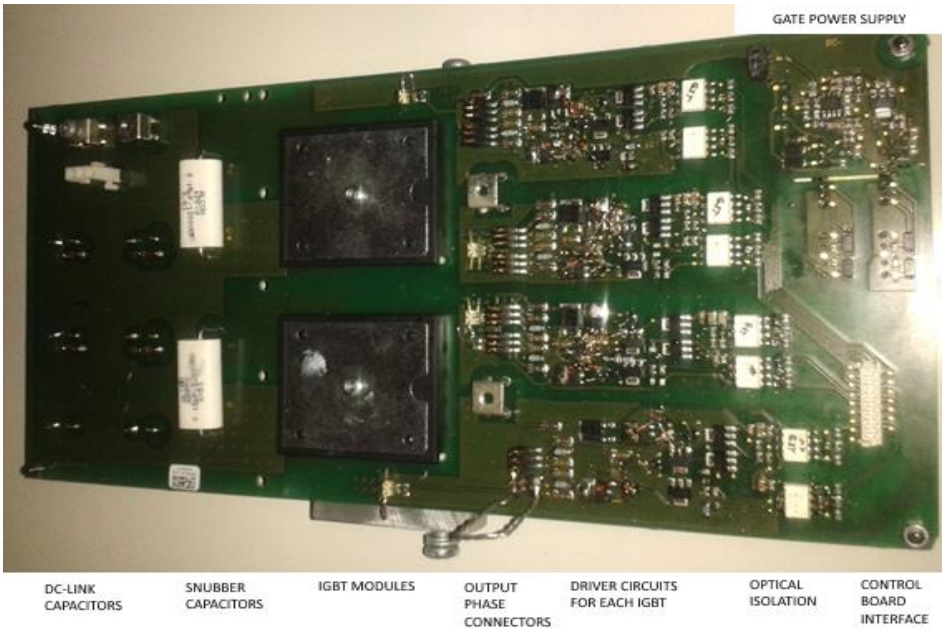

Figure 28. *The power board with the final modifications.*

On the power board there is also a power supply for the gate drivers that requires an auxiliary +15 V_{DC} isolated supply. High-side drivers need to be isolated from the DC bus potentials. The DC capacitors of the main circuit can be either soldered to the board or connected to the screw terminals located on the top-left corner on the DC-link's side of the board. An external high voltage DC power supply is used for the main circuit.

3.2 Schematics design

The final schematics is included in Appendix J. The component references related to the driver circuit in the following chapters are referring to the U_LO driver schematics, found on the appendix sheet U_LO_DRIVER. The component-specific functional descriptions are found in Appendix A. The schematics of the gate power supply shall not be introduced in this thesis and the related sheets are not included in the schematics.

3.2.1 Control board

The control board is used as a simple user interface and precise timing signal source for laboratory use. It was designed to be used for also other IGBT module testing prototypes, which together with safety reasons justify the mechanical separation. The other driver boards would only need to host an input connector for the signals. Since the control board is not in the main scope of the study, it will be left for a fairly low attention.

CPLD interface

The additional CPLD board provides the needed precise timing for the IGBT measurements and simulates the fault recognizing logic of a real frequency converter. The CPLD board hosts an Altera MAX II EPM240 CPLD, a 50 MHz clock oscillator, a programming connector and a 3,3 V_{DC} power supply. The CPLD board is attached to the control board by female headers (connectors X2 and X3). The schematics of the interface are included on page 1 in Appendix J.

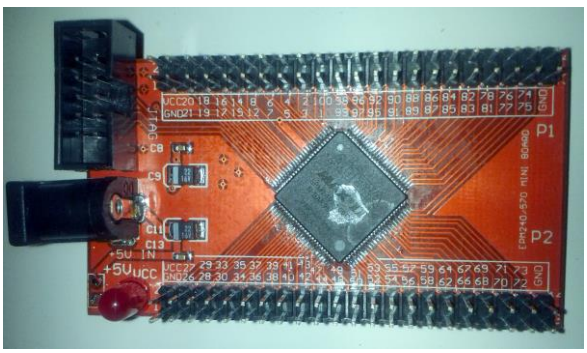

Figure 29. *CPLD evaluation board*

The reason for selecting this external board instead of integrating the logic on the control board was the easiness of its use, an existing basis for the code and a possibility to swap the CPLD boards in case of comparing two different codes or damaged board. These boards have already been in use when studying the behavior of IGBTs. The CPLD is controlled via a simple user interface that is located on the control board and consists of six programmable switches (S1-S6). In addition to the switches, there is a male pin header X9 for easier measurements of the output signals.

Voltage to current signal conversion circuitry

The CPLD uses +3,3 V_{DC} supply voltage that is formed with a linear regulator on the CPLD board. The low voltage with the limited current sourcing/sinking capability of the CPLD force to use a voltage level conversion circuitry on the board. The optocouplers (Avago Technologies HCPL-J314) need an input current of 8…12 mA for proper switching. The forward voltage of the optocoupler's diode is specified as 1,2…1,8 V_{DC} with 10 mA current. [2] The CPLD can sink and source maximum of 25 mA, but the output voltage swing may be limited to 0,45…2,4 V_{DC} (LVTTL) or 0,2…3,1 V_{DC} (LVCMOS), depending on the used output configuration. This might lead to improper or delayed switching. Also limiting the current to a desired value would be insecure due to relatively loose supply voltages. [13] The chosen signal levelling circuitry in Figure 30 bases on NPN transistors that use CPLD's output signals as their inputs.

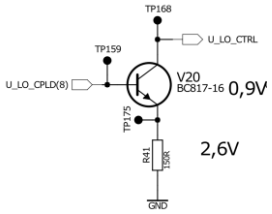

Figure 30. *Schematics of signal conversion circuit for U_LO*

The current limiting is done with a *current sink*. [21] The current sink converts the CPLD's +3.3 V_{DC} output signal to a 17 mA current signal for optocoupler and its bypass resistor. Slew rate of optocoupler's input voltage with the transistor circuit is about 30 V/us. The parallel 220 pF capacitor on optocoupler's input slows down the switching but is essential to prevent false switching signals from occurring.

Connection between control and power boards

The signals from the control board to the power board are delivered as two-wire current signals as marked in Figure 31. Each signal uses its own +5 V_{DC} line that is not connected

to other supply lines on the power board. This minimizes the inductive coupling of interference due to reduced current loops, interference caused by a shared impedance, and voltage losses on the lines, thus making the signaling circuit more tolerant for external interference. Previous gate driver designs have revealed some problems in the signal delivery, when the gate signals have shared a common supply or return line with larger current loops between wirings.

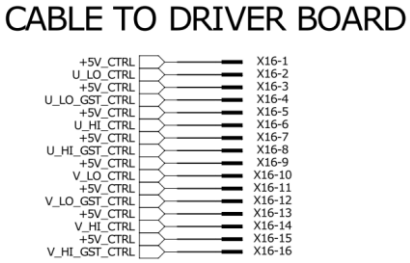

Figure 31. *Schematics of control board driving signal connector*

As a downside of this solution, the numbers of signal cables and connector pins are increased. This may increase the component cost and failure rate, as well as make the routing more difficult due to lower flexibility of the cable. For testing purpose, however, using this kind of setup was seen advantageous.

3.2.2 Driver circuit

This chapter will focus on the driver-related circuits located on the power board: optical isolation, boosting circuits, current amplifier, gate resistors and auxiliary gate capacitor. Since the schematics are equal for all the four driver channels, only U_LO is introduced.

Optocouplers

The high-side drivers need to be isolated from DC-, because the high-side IGBT's gate voltage is referenced to the high-side IGBT's emitter. To keep the signal delays and thermal behavior similar between high- and low-side drivers, also the low-side drivers use optocoupler isolation. This helps in avoiding interference caused by IGBT's switching and conducted backwards to the control circuit. Secondly, it gives possibility to use the DC-link as floating, i.e. without connection to supply grid's protective earth (PE).

The single-channel optocoupler chosen for the prototype is similar that the ones used in the company's commercial gate drivers. If offers relatively good output current characteristics, ability to work with +/– 15 VDC supplies and sufficient delays and isolation capabilities. For GST driver use, having two channels would be advantageous, though.

Boosting circuits

A capacitive boosting circuits were applied on two locations in the driver to increase the switching speed and to decrease the total delay. The circuits consist of parallel RC circuits. The related components are highlighted in Figure 32. The current sink/source between the optocoupler and the push-pull transistor stage on the output is called *pre-driver*. It is used for driving the output stage transistors with a constant current.

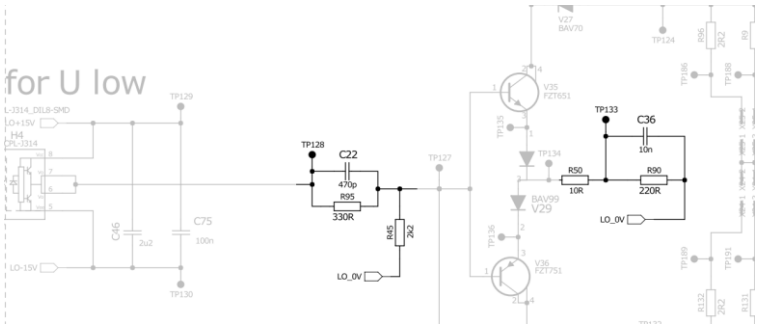

Figure 32. *Boosting circuits on the optocoupler's output and on the pre-driver's current sink*

In the pre-driver's current sink, there is also a current limiting resistor R50 to prevent the saturation of pre-driver transistors during switching. On the optocoupler's output the current is not locally limited, but since the current path goes through R50, it will simultaneously limit the optocoupler's output current from exceeding the maximum ratings. R45 near the optocoupler's boosting circuit is used for setting the steady-state level of pre-driver's input voltage. During on-state, the resistors R95 and R45 form a resistive voltage divider. The excess voltage is lost in the resistance of R95, preventing the pre-driver transistors from entering into saturation.

Desaturation circuit

To make the gate driver fast enough, transistors in driver and pre-driver should never be let into a state of deep saturation. Recovering from saturation is a slow process, which causes increase in losses in push-pull stage and in IGBT. When a saturated push-pull stage is switched, the current will flow straight from the positive to the negative supply through the gate resistors. This causes slowly changing gate voltage and therefore also increased losses in the IGBT.

There are several ways to limit the operation of bipolar junction transistors in the push-pull stage to stay on the active region. The used circuitry, Baker's clamp in Figure 33, is based on controlling the source of current that is fed to the pre-driver's constant current

sink. During normal operation, the current generator obtains its current partly from +15 V through 330R resistor R133 and partly through the base of V34 and resistor R147. The current is led through diodes in V16 and the diode located between pins V27:2 and V27:3. The diodes cause a voltage loss of ~1,2 V, and because the resistance of R147 is fairly low, the base voltage is around 1,4 V above the collector of pre-driver transistor V35. When the IGBT is turned on, the pre-driver's collector voltage is around 13…13,5 V.

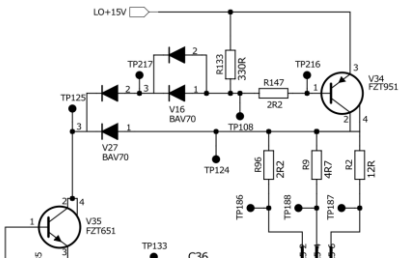

Figure 33. *De-saturation circuit in U_LO gate driver*

When the driver transistor V34 conducts current, its collector potential is dependent of the control (base current). The current of pre-driver is designed to be high enough to force V34 into saturation in steady state. Lower currents of pre-driver would have caused increase in delay. When V34 approaches saturation region, its emitter-collector voltage decreases to ~1 V, letting the collector rise close to 14,5 V, the pre-driver starts to obtain current from the collector of V34. Because pre-driver is a constant current sink, this causes a reduction of base current and prevents the driver transistor from entering into saturation. When the IGBT's gate is turned on, the steady state voltage of the collector of driver transistor is around 14,5 V. This is because of the positive supply voltages that are slightly above 15 V.

Two diodes are needed in series to gain margin for the transistor's operation. The prototype was first tested with only one diode in series, which caused V34 to saturate. It was noticed that the collector-emitter voltage difference has to be higher than the base-emitter voltage difference. The second diode causes an additional 0,5…0,6 V voltage drop for the line between pre-driver transistor's collector and driver transistor's base. This makes sure that the base of V34 stays always at a higher potential than the collector. It should also be noted that adding diodes from driver transistors' collectors and pre-driver transistors' collectors to +/– 15 V supply may be useful to protect the circuit from interference.

Gate resistors

The gate voltage curve can be adjusted by changing the gate resistor values. To make the gate resistor adjustment as flexible as possible, the driver's should be able to output as high current with as high slew rate as possible. In the IGBT modules, there may be several

parallel IGBT chips, and therefore also several individual gates that are wanted to be controlled simultaneously. The reason for this is the need for larger currents, which is achieved by increasing the number of individual chips rather than the size of one chip. Using parallel chips creates a need for balancing, which in Semikron's IGBT modules is done by adding an internal resistor for each IGBT chip. See Figure 34 for details. [9] The balance between chips is important for even distribution of heat and the prevention of ringing between the gate capacitances of IGBT chips and the inductance of the wire connecting them. In the used IGBT module, SKiiP 24GB12T4V1, the total parallel resistance of internal gate resistors is 5 Ohms.

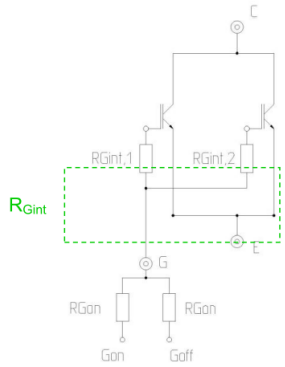

Figure 34. *The internal structure of Semikron's MiniSKiiP Generation II IGBT module [9]*

Due to the use of internal gate resistors, the possibilities of adjusting the switching characteristics with external gate resistors is limited. Since the purpose of testing this driver prototype was to find out its capabilities, a low turn-on and turn-off resistors were used. Both were chosen as 1 Ohm resistors to achieve high currents through push-pull transistors. Lower values would not significantly affect the switching characteristics, but might stress the other parts of the driver circuit unnecessarily. On the other hand, allowed EMI levels limit the need for extremely fast switching so that gate resistors with a value lower than 1 Ohm are rarely used.

Soft turn-off circuit

The previously introduced push-pull –type gate driver offers a platform for functionality that is used for slowed turn-off of the IGBT during a fast, high-current short circuit on the output phases. The caused turn-off overvoltage can be reduced by slow switching procedure, which is based on discharging the gate capacitance through a resistance that is remarkably higher than the normal turn-off gate resistance. The final assembly of the gate driver is included in Figure 35.

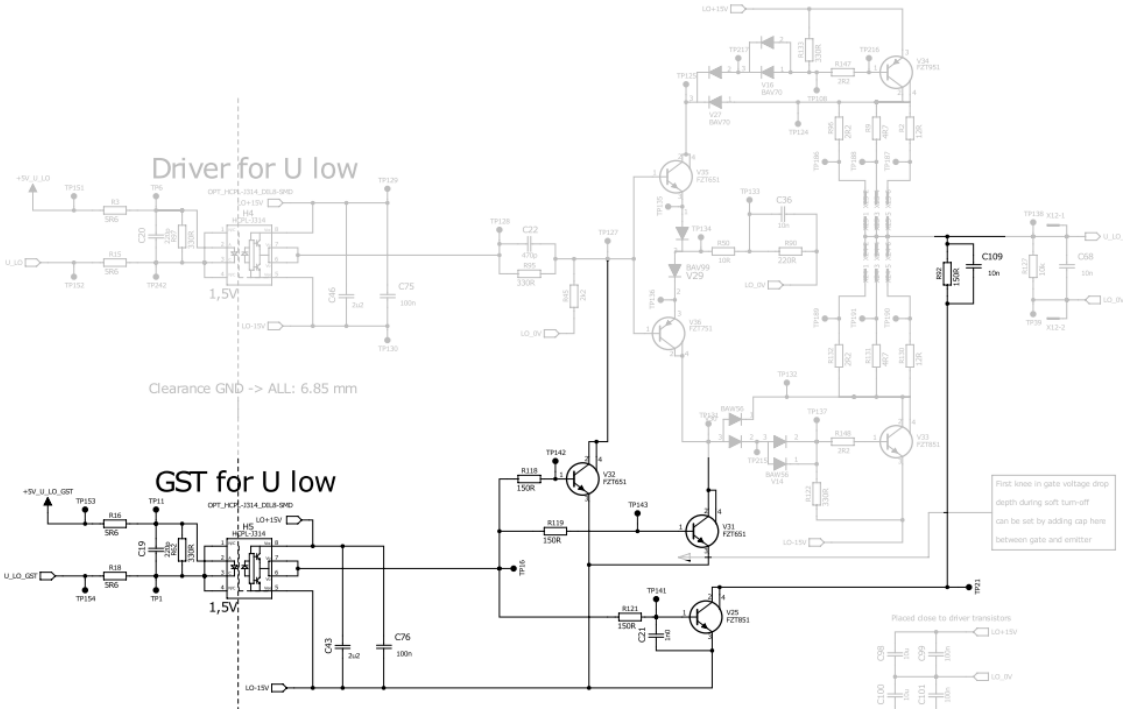

Figure 35. *Schematics of U_LO driver circuit with added Gate Soft Turn-off circuitry*

The GST functionality developed for the prototype is an optional function. The driver can be used with or without GST circuitry. On the other hand, GST circuitry can be implemented also to other drivers with same kind of topology. The same need for isolation is valid for the high-side GST circuits as is for the high-side drivers. Also for the GST circuits the optocouplers were added for all channels.

When GST function is enabled, the corresponding pin on CPLD will set and cause the optocoupler on GST line to activate. After optocoupler's output has changed its state, GST transistors will start conducting. Two of them cut the normal gate driving signal route. The third one connects the IGBT's gate to -15 V supply through a resistance that has a small capacitor (nominal value ~10 nF) connected in parallel. The capacitor causes a capacitive voltage divider to drop the first step of gate voltage, being some volts of amplitude. Purpose for this is bringing the IGBT to the linear region to quicken the start of turning off. The behavior is relatively similar to the boosting circuit used in the driver.

3.2.3 Main circuit

The main circuit of the prototype simulates the INU (inverter unit) of a frequency converter. The DC link capacitors are included on the PCB. Alternatively an external capacitor can be used. The main circuit components were selected by main circuit development engineer Jari Koljonen. The selection was made in order to provide information for one on-going development project.

To simulate the real switching scenario, the operation was verified with a dual-pulse test. A load current of ~150 A was switched between free-wheeling diode and the IGBT. The turn-off switching behavior was measured in the end of the first pulse, while the turn-on was measured in the beginning of the second test pulse. The measurement procedure follows the guidelines recommended by the IGBT module's manufacturer. [11]

Snubber capacitors

IGBT switching causes a short-term high current pulses to the DC-link. To reduce the induced voltage ripple peaks, snubber capacitors are placed as close as possible to the IGBTs to minimize trace/bus inductance. Without snubber capacitors, the stray inductance of DC bus copper planes and main DC capacitors would cause overvoltage peaks over the IGBT during IGBT's turn-off.

On the prototype there are places for two snubber capacitors for each module, but only one per module is assembled at once. The places are equipped with different pitch for testing purposes. In the final assembly, a pair of ALCON KPF-9 0.15 uF / 1200 VDC capacitors was used. Choosing optimal snubber capacitors for a power board needs taking account various factors, such as properties of main DC capacitors', DC bus, IGBT and the overall layout of the main circuit. It is usually done by the main circuit designers.

DC-link capacitors and discharging resistors

Six pieces of custom-made 180 uF electrolyte capacitors (Epcos B43624-B5187-M, 180 uF / 450 V) in two-level topology in DC-link sum up to the total capacitance of 270 uF and withstanding voltage of 900 V. [10] During turn-off overshoot measurements, the through-hole –type (*THD*) capacitors were removed from the PCB and an external 700 uF / 900 V custom-made capacitor was connected on the screw terminals X5 and X10.

As the built prototype board is for laboratory use, there is no safety specification for the discharge time of the main DC-link capacitors. The selection of the discharging resistors was made in effort to find a reasonable discharge time and keep the power loss of the resistors during on-state at a moderate level. The discharging resistor selection follows the practice of previous prototypes. [10]

3.3 Thermal limits of the driver

The table of driver circuit components' thermal limits is included in Appendix B. The table is formed by using the absolute maximum values of datasheets and by derating them according to factors that are commonly used in industry. The maximum temperature allowed in the board space inside the frequency converter is limited by the derated ambient

temperature for the optocoupler HCPL-J314, which is 80 °C. In temperatures above this, the optocoupler may not work as intended or its lifetime may be limited. In board space temperatures under 80 °C, it has to be taken into account that the maximum power dissipation of the components does not exceed their derated values.

According to simulations, only one component in the driver circuit doesn't fulfill the requirement for derated power. The component is R90 (in U_LO driver), a MELF power resistor in the pre-driver's current sink. It exceeds the derated maximum power by 20 mW. Therefore it would be useful either to use two MELF resistors in series or in parallel, or place an additional 1206 chip resistor in series with R90. In that scenario, the resistance of R90 should be decreased by the resistance of added chip resistor. It should also be noted that the base resistors R118, R119 and R121 in the GST circuit are only used for some or some tens of microseconds during activation of GST function. Their maximum peak pulse power is ~5,6 W, and therefore they would not last long GST pulses. The pulses are limited by the CPLD logic.

3.4 Layout design and clearance distances

The layout was done by following general driver layout considerations. [12] The main focus was put in the minimal use of PCB area and fulfilling safety requirements. The *creepage distances*, meaning the isolation distances between different nets on the PCB, were chosen to fulfill the requirements given by standard IEC 61800-5-1 for a frequency converter with a diode rectifier input bridge and three-phase 400 V_{AC} input [9]. The distances are not standard-compatible when performing turn-off overshoot measurements, but are still well sufficient to prevent shoot-throughs. The used creepage distances were set to class rules of PADS.

The layout work was done by using PADS Layout and routing by using PADS Router. The masks and assembly drawings for the PCB are included in Appendix K and Appendix L. It should be noted that the files are the original ones, used for manufacturing the prototype. Some components and traces have been modified during the development.

3.5 Reference design

To clarify the qualities of the studied driver circuit, another IGBT gate driver was used as a reference for comparison. *The reference circuit* is presently used in some of the company's frequency converters. The selection of reference driver was mainly based on the fact that there was a prototyping board available for the same IGBT module which also the studied driver was using. Because the driver's output values depend on the driven IGBT, using similar IGBT module as a load for the driver is beneficial for comparability. Both of the drivers also use the same optocoupler for isolation and have BJTs as their driver transistors. The schematics of the reference driver is included in Figure 36.

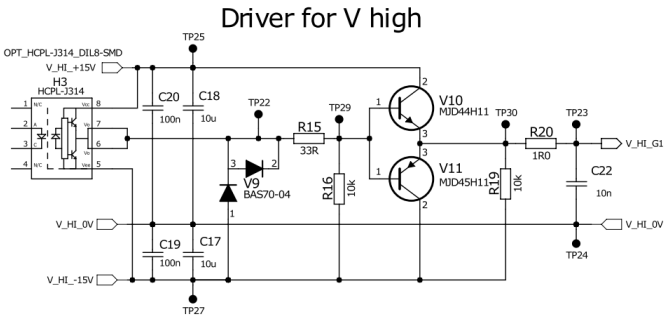

Figure 36. *Schematics of the reference driver*

The chosen driver is not an optimal solution as reference, since it is designed for lower-current IGBTs than the studied driver. The driver transistors MJD44H11 and MJD45H11, however, are high current models that offer 16 A peak current. Their current supplying capability makes them therefore comparable with the transistors of the studied driver, FZT851 and FZT951, whose peak collector current is 20 A (FZT851) and 15 A (FZT951).

The difference between the drivers is that the reference driver does not include a pre-driver or boosting circuits and that the transistors are connected as a so-called *totem pole* configuration. The gate resistor R20 is also shared for turn-on and turn-off. Transistor V10 is used for turn-on, V11 for turn-off. R15 limits the current through the transistors during switching. R16 and R19 are used for ensuring that the IGBT stays non-conductive in case of optocoupler failure and when the gate power supply is turned off. C17-C20 are supply filter capacitors, and C22 is an auxiliary gate capacitor. To make the comparison feasible, similar main circuit construction and gate power supply were used for both drivers. Also the gate resistor and auxiliary gate capacitor values were similar for both drivers.

3.6 Measurement setup

This chapter introduces the measurement equipment and auxiliary main circuit components. Also the reasons for using certain data handling procedures are explained. As the oscilloscope channel setup changed between most driver circuit measurements, they have to be introduced before each result presentation.

3.6.1 Used equipment

For dynamic driver analysis, a 300 MHz Tektronix DPO3034 was used with passive voltage probes Tektronix P6139A (500 MHz, 300 V, 10:1) and an active current probe TCP0030. The oscilloscope was connected to a PC for transferring the data. For main circuit measurements, a 500 MHz Tektronix DPO7054 digital oscilloscope was used with Tektronix THDP0200 differential high voltage probes and 1,2 kA CWT 6B UM Rogowski current transducers. DPO7054 offers higher sampling rate than DPO3034, better usability and has a better software that allows combining the results from different

measurements to the same image. The data from main circuit measurements was mainly handled on the oscilloscope. All the measurement equipment except the 30 A active current probes were calibrated by an authorized company within a year before the use.

The used low-voltage power supplies were generic Mascot DC supplies. For high voltage measurements, a Testcom LPS 750-HV adjustable HVDC voltage supply was used. It is capable of providing 1250 VDC and 1 A for the load. For thermal analysis of driver circuit, a temperature controlled test cabin Thermotron S-1.5-3200 was used. The thermal behavior of the IGBTs were tested by installing the IGBT modules' heatsink on a heat plate Torrey Pines Scientific HP30A-2.

Two different air-core coils were used as load for main circuit testing, because such coils can stand vast currents through them yet still maintaining their linearity. The inductance of the large coil was 69 μH and it was used for simulating inductive motor load during normal switching. The inductance of the smaller coil one was 1,5 μH. It was used for testing soft turn-off function and represented a hard short circuit. The inductances of the coils were measured with an Agilent U1731A inductance meter.

To make the effects of soft turn-off circuit better visible, the snubber capacitors were removed from the board. This causes the recovery voltages to increase significantly even under normal operation conditions. Although the setup no longer simulates the main circuit of a frequency converter accurately, it was seen beneficial in clarifying the operation and advantages of GST function.

3.6.2 Probe calibration

Due to the use of different types of probes and the need for accurate timing of waveforms in main circuit measurements, it was necessary to calibrate the propagation delays of Rogowski coils and differential voltage probes to match each other. Without calibration, a difference in the propagation delays would cause severe inaccuracy for the switching energy calculations. Propagation delay was set to zero by driving a test pulse through a 25 Ohm very low-inductance dU/dt resistor connected between DC+ and an output phase IGBT U_LO. This means that with fast transients, the current through the resistors follows accurately the voltage applied on the resistor. Voltage and current waveforms on the resistor were simultaneously recorded on the oscilloscope and the waveforms were set to be timely equal. The calibration was done by adjusting the deskew value on the oscilloscope. Measurement parameters are listed on Table 2. Calibration result is included in Figure 37.

Table 2. *Setup in deskew calibration*

Parameter	Value
DC-link voltage	200 V
Pulse 1	4 us
Interval between pulses	9 us
Pulse 2	10 us
Calibration trigger	Falling edge
Calibration value for deskew	34 ns

Figure 37. *Propagation delay calibration measurement with a differential voltage probe and a Rogowski-type current probe*

Due to ringing in the waveform during rising edge, it was regarded more reliable to perform calibration using the falling edge of the signal. The amplitude of ringing was significantly lower on the falling edge.

3.6.3 Data handling

The results from the most measurements regarding the driver and the main circuit were saved in two or three different formats, including .png image, .wfm waveform and .csv data. The .wfm is a Tektronix-specific format that saves the data of measurement's setup, timing and values. It can only be read by Tektronix' own software and the oscilloscope. The advantage of using .wfm is that the data from previous measurements can be brought to the oscilloscope screen as a reference waveform and handled as a fresh result, which makes comparing results from different setups easier. It is also possible to convert .wfm files to .csv, which was done for some results to make data handling and drawing graphs in Excel possible. Some results were saved as .csv already with the oscilloscope.

For driver measurements conducted in a low-voltage setup the statistics function of the oscilloscope was used as an additional data handling tool. The statistics give information about variation in signal levels and delays. To gain enough data, sequential driving commands had to be given for the driver and additional hardware was considered the easiest way to perform it. The setup consists of a microcontroller board (Arduino Mega 2560) loaded with a code that produces 100 pairs of sequential RESET and START pulses to CPLD's input pins, causing the gate driving signal to be triggered 100 times in a row. The oscilloscope saves the waveforms and gathers information for the given measurements. The data is valid only for the last 100 pulses, since the oscilloscope statistics were reset after every measurement. By observing the standard deviation and mean, the varying of the signal delay/amplitude can be monitored.

The waveforms drawn to the oscilloscope screen are not waveforms of one pulse, but averages of 16 last triggered signals. This was used to filter random interference from the signal. The practice was tested with some single-triggered reference captures, but the main features in the curves (overshoots, signal levels, rise times, ringing) were repeated well. Using the average instead of single-triggered captures helps to distinguish whether an uncommon shape on a waveform is present repeatedly or not. "*Value*" (also found in the measurements window) is a mean of the samples drawn to the screen. Difference to "*Mean*" in the measurements window is that "*Mean*" uses data of last 100 samples. The averaging and statistics do not give reliable data under all circumstances. If the waveform contains severe ringing on its rising edge, the triggering and calculation points may vary between pulses. This should be kept in mind when interpreting the statistics data.

4. RESULTS AND DISCUSSION

This section introduces the measurement results and interprets their critical qualities. It compares the results against the requirements, datasheet values, and the expectations from simulations. Some values are also compared to the results gained with the reference design.

The measurements were started with power supply voltages as they affect to the IGBT's switching behavior by setting levels for the gate voltage. The booster circuits were measured to justify their additional components. As the driver transistors' saturation would cause increase in the gate power consumption and affect the gate voltage by slowing the transistors' turn-off, it had to be verified that the desaturation circuit is operating properly through the temperature range. The delays and jitters were measured to ease the comparison between different driver circuits. High jitter levels might reveal problems with interference or poor design, thus making the driver unsuitable for some applications. On the other hand, measuring delays and jitters separately for each functional block on the driver, the source of the delay could be found and possibly eliminated or adjusted. Finally, the output currents and voltages of the driver were measured to verify that the driver is able to supply desired voltage and current values. The values are comparable with other drivers when the rest used test setup is taken into account. When observing the behavior of the output, also the effects of auxiliary gate capacitor were studied to find ideal value for it. The source material was not handling the value selection thoroughly enough.

Information about the driver's actual capability was obtained by observing the switching behavior of the driven IGBT for both normal and soft turn-off switching. Well-adjusted, high performance driver circuit would cause lower losses, which affects the need for cooling and again to the power consumption and costs. Although the results are applicable only for a certain driver – IGBT –combination, the output behavior could reveal problems with the driver's supply capability. The soft turn-off measurements with different R_{GST} and C_{GST} values were needed for finding a proper value combination as the main circuit behavior cannot be easily simulated. As the driver is supposed to operate as expected through the temperature range, its operation had to be tested by using a heated test cabin. This also gave information about the most temperature-dependent functional blocks of the driver, thus helping to design enhancements.

The following results focus on the results achieved with the final driver setup, whose schematics is included in Appendix J. Unless otherwise mentioned, they are all measured at 25 °C ambient temperature after stabilization of the prototype board temperature. As

the scope of the study is the driver circuit and main circuit phenomena, the behavior of control board is not introduced in detail.

4.1 Driver circuit

The measurements needed for adjusting the driver were performed without HVDC power supply on main circuit. Later it was verified that the effects of main circuit were not conducted backwards to the driver circuit. The effect was limited to the driver output, i.e. gate voltage and current. Final delays were measured with a 620 V DC-link voltage.

4.1.1 Power supply voltages

In the beginning of measurements, steady-state voltages were measured by using a Fluke 179 multimeter. Results are included in Table 3 and refer to schematics of Appendix J.

Table 3. *Steady-state supply voltages on the driver circuit*

Supply net	Value, V	Reference net
+5 V_{IN}	5,61	GND
+15 V_{IN}	14,93	DC-
LO_+15V	15,15	LO_0V
LO_-15V	-14,69	LO_0V
U_HI_+15V	15,08	U_HI_0V
U_HI_-15V	-14,84	U_HI_0V
V_HI_+15V	15,06	V_HI_0V
V_HI_-15V	-14,85	V_HI_0V

As can be seen on the results, the gate supplies are slightly unbalanced. Since the switching behavior is mainly characterized by the positive supply level, the results are considered representing the use of +15 V_{DC} supplies. Normally a tolerance of ± 5 % is allowed for the gate supply voltages.

4.1.2 Characteristic behavior

In this section, the operation of the driver circuit is verified. The focus is on the subcircuits that cause the studied driver to differ from other push-pull or totem pole drivers.

Pre-driver's boosting circuit

Figure 38 visualizes the turn-on characteristics of pre-driver circuitry with the oscilloscope channel setup of Table 4. The test points refer to the U_LO driver schematics found

on page 2 in Appendix J. It can be seen from the graphs that the steady-state voltage loss over resistor R50 is around 0,6 V. As R50 is a 10 Ohms resistor, the current is ~50…60 mA. Since the same current is going also through 220 Ohm resistor R90 in steady state, R90 generates significant amount of heat. Simulations give an approximation of ~520 mW, which is supported by measurements. 50 mA constant current would produce about 550 mW of power loss in the resistor, which means it should be assembled as one or two MELF resistors or large surface mounted (*SMD*) chip resistors. The power loss on R90 is relatively steady, because the peak current during switching passes by R90 through the capacitor in parallel to it and the steady-state current is symmetric for both on- and off-states. Long-term temperature difference, *dT*, was measured to be ~40 ‘C, when a constant driving signal of 10 kHz frequency was set as an input for the driver circuit.

Table 4. *Setup in measuring*

Oscilloscope channel	Point of measurement	U_LO test point	Reference net
CH3	Optocoupler’s output	TP128	LO _0V
CH1	+15 V / -15 V	TP129 / TP130	LO _0V
CH2	Pre-driver’s current sink resistor R50:2	TP133	LO _0V
CH4	Pre-driver’s current sink resistor R50:1	TP134	LO _0V

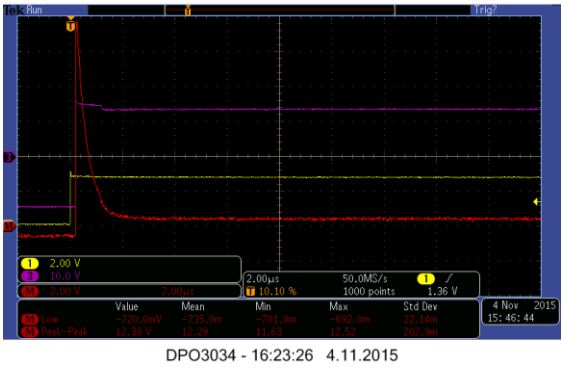

Figure 38. *Pre-driver’s operation with C36 assembled.*

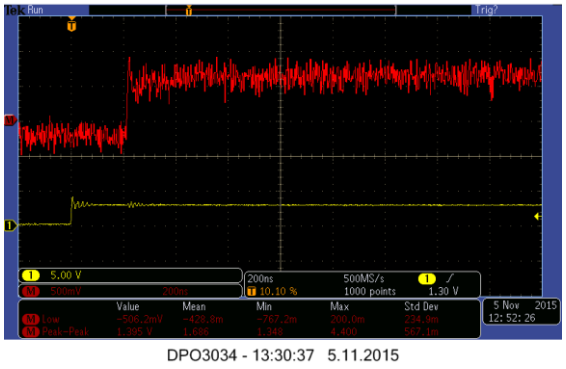

Figure 39. *Pre-driver’s operation without C36.*

During turn-on and turn-off, the capacitor C36 causes a peak in the pre-driver current. The peak voltage over R50 is ~13 volts, which translates into a 1,3 A current and ~17 W peak power. Even if the pulse lasts only for less than 0,5 us, R50 should be assembled as a pulse resistor, preferably MELF. The function of C36 is to drive a high current peak to the gate, causing faster switching and lower losses. Figure 39 visualizes the circuit’s operation without capacitor C36 during turn-on. No peaking in the current waveform is pre-

sent. Note that the voltage scaling is changed. For the driver's output, the effect of capacitor C36 can be seen from Figure 40 and Figure 41. Table 5 presents the used oscilloscope channel setup. The test points refer to the U_LO driver schematics found on page 2 in Appendix J.

Table 5. *Oscilloscope channels when measuring the effect of boosting circuit in pre-driver to the driver's output*

Oscilloscope channel	Point of measurement	U_LO test point	Reference net
CH3	Optocoupler's output	TP128	LO _0V
CH1	CPLD pin	TP159	GND
CH2	Turn-on driver's collector	TP124	LO _0V
CH4	Pre-driver transistor's collector	TP125	LO _0V

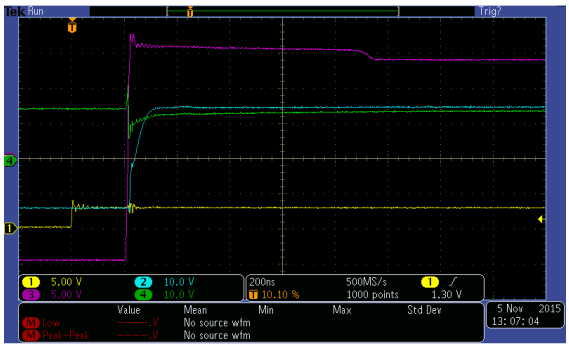

Figure 40. *Driver's operation with C36 assembled*

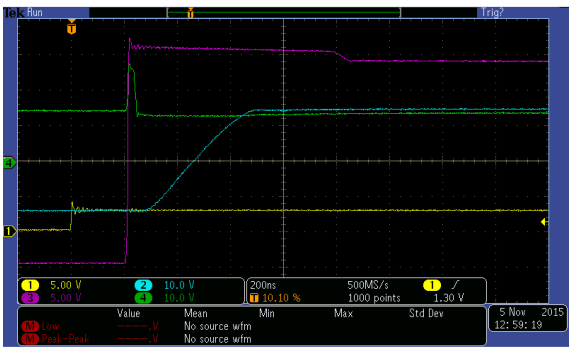

Figure 41. *Driver's operation without C36*

With C36 assembled, the gate voltage (CH2) increases fast, in less than 100 ns. The step from -14 V to -2 V is steep and starts immediately after the optocoupler's output has changed its state to high level. After that the gate voltage slope is ~300 V/us. When C36 is disassembled from the circuit, a delay of ~100 ns appears in the beginning of gate voltage slope. Also the slope is lower, ~70 V/us.

Optocoupler's output boosting circuitry

Figures 42 and 43 show that C22 is used for balancing the effect of C36 through a capacitive voltage division. Table 6 introduces the used oscilloscope setups. The test points refer to the U_LO driver schematics found on page 2 in Appendix J. With C22 assembled

(setup [1]), the voltage loss over the RC circuit at the optocoupler's output is ~10 V. If C22 is left out of the circuit, C36 represents a short circuit and almost all of the 30 V transient is left over resistor R95 at the optocoupler's output. Resistor R95 limits the current to the predriver and therefore slows down the start of the switching event. This can also be seen in the driver's output which are presented in Figures 44 and 45 with oscilloscope setup [3] of Table 6. In both cases the 22 nF capacitor C36 is assembled in the predriver's current sink.

Table 6. *Oscilloscope channel setups when measuring the effect of boosting circuit in optocoupler's output*

Oscilloscope channel setup [1]	Oscilloscope channel setup [2]	Oscilloscope channel setup [3]	Point of measurement	U_LO test point	Reference net
n/a	CH1	CH1	CPLD pin	TP159	GND
CH3	CH3	CH3	Optocoupler's output	TP128	LO _0V
CH1	n/a	n/a	+15 V	TP129	LO _0V
CH2	CH2	n/a	Pre-driver's current sink 10R resistor	TP133	LO _0V
CH4	CH4	n/a	Pre-driver's current sink 10R resistor	TP134	LO _0V
n/a	n/a	CH2	Turn-on driver transistor's collector	TP124	LO _0V
n/a	n/a	CH4	Pre-driver transistor's collector	TP125	LO _0V

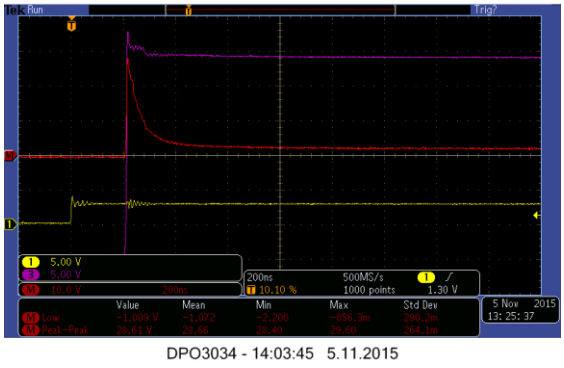

Figure 42. *Operation of optocoupler's output with C22 assembled. Oscilloscope channel setup [1].*

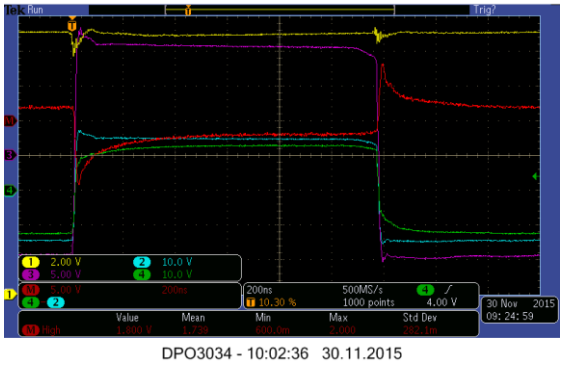

Figure 43. *Operation of optocoupler's output without C22. Oscilloscope channel setup [2].*

Figure 44. *Operation of driver's output with C22 assembled. Oscilloscope channel setup [3].*

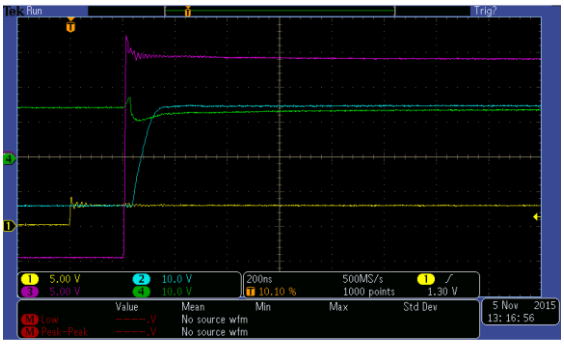

Figure 45. *Operation of driver's output without C22. Oscilloscope channel setup [3].*

The effect of C22 to the gate voltage is the first step from -14 V to -4 V in the gate voltage curve. The slope after the step is steady ~300 V/us with both circuits. The delay caused by removing C22 is ~20 ns, which is significantly shorter than the delay caused by removing C36. Note also the change in the optocoupler's output curve (CH3). In Figure 44, the output stays above the optocoupler's supply, at ~16,5 V, for 800…900 ns. After removing the C22, the output stays at ~14,5 V, if the small overshoot is neglected. This was traced to be caused by the optocoupler's internal circuitry. With high output current, the output voltage is kept at a higher level, possibly to quicken the switching process. When C22 is removed, the output current does not have a start-up peak, and the output voltage is not boosted. There is no mention about this function in the datasheet.

Desaturation circuit

Behavior of saturated push-pull transistors is included in Figure 46. The used oscilloscope channel setup is given in Table 7. Test points refer to schematics in Appendix J. The first peak is the turn-on switching, the second one is a waste pulse during turn-off switching, caused by simultaneous conduction of both turn-on and turn-off driver transistors.

Table 7. *Oscilloscope channels when measuring transistor saturation*

Oscilloscope channel	Point of measurement	U_LO test point	Reference net
CH3	IGBT's gate voltage	TP138	LO _0V
CH2	+15 V	TP129	LO_0V
CH1	Turn-on driver's collector voltage	TP124	LO _0V
CH4	Turn-on driver's collector current	n/a	n/a

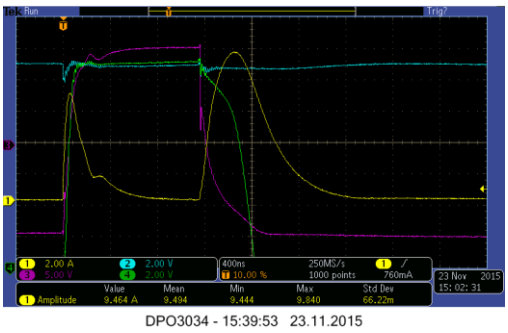

Figure 46. *Driver output characteristics with saturated push-pull transistors*

Due to non-ideality of transistors, a waste pulse was still present in the current waveforms after implementing the desaturation circuit. The amplitude, however, was decreased to around 25 % of the proper collector switching current. The results are found in Figure 52.

4.1.3 Delays

The first two measurements are conducted for all four driver channels, but since no significant differences could be seen, oscilloscope screen captures of only U_LO driver are presented. Later measurements were continued with two channels, U_LO and V_HI.

CPLD pin – optocoupler's input

The delay from the CPLD to the optocoupler's input was measured for calculating the actual driver's delay and to distinct that from the delay of the optocoupler and the control circuit. The result is presented in Figure 47 with an oscilloscope setup of Table 8. The test points refer to the U_LO driver schematics found on page 2 in Appendix J.

Table 8. *Oscilloscope channels when measuring delay between CPLD and optocoupler's input*

Oscilloscope channel	Point of measurement	U_LO test point	Reference net
CH1	CPLD pin	TP159	GND
CH2	Signal conversion transistor's emitter	TP175	GND
CH3	Optocoupler's input, anode	TP6	GND
CH4	Optocoupler's input, cathode	TP242	GND
Math (CH3 – CH4)	Voltage loss of optocoupler's input	TP6 -> TP242	n/a

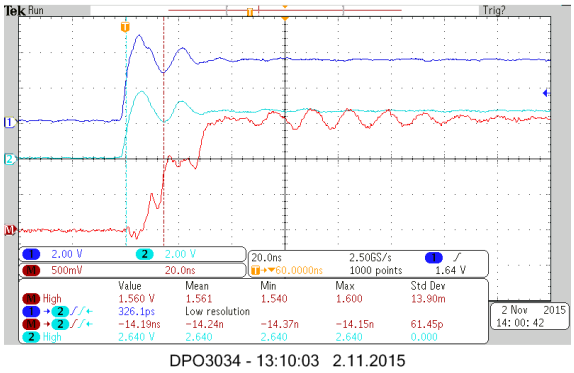

Figure 47. *Voltage waveforms of CPLD pin and optocoupler's input in U_LO driver channel*

As seen on Figure 47, the rise of CPLD's pin is steep and the signal conversion transistor's output current follows it tightly. Rise times are 2-3 ns and variation is negligible. Delay from CPLD's pin to signal conversion transistor's output is only ~200 ps. The oscilloscope's measurement precision limits the accuracy of fast rising signals, since the rising edge is drawn by only 4-8 data points.

The rise time of optocoupler's input voltage is significantly higher, around 35 ns. This is partly caused by wire inductances, partly by the capacitor in parallel with the optocoupler. Also the LED on the optocoupler's input is a non-linear component, making it hard to distinguish the actual turn-off moment of the optocoupler. The inductances could be significantly higher if the paired signal wires between control board and power board were kept separate or the signals of different phases shared a common return line. Also the interference would probably be higher in amplitude.

The delay from signal conversion circuit to optocoupler's input (90 % of end voltage) varies between 30-35 ns. No significant variance between different channels could be seen. On the other hand, the optocouplers installed on the board are probably from the same batch, causing their characteristics to be similar with each other. The 60-70 MHz ringing in the curves is mainly caused by common mode noise of switching.

Optocoupler's propagation delay

The waveforms of Figures 48 and 49 reveal that the delay caused by optocoupler is multiple times longer than the delay caused by its input driver circuitry. The oscilloscope setup is introduced in Table 9. The test points refer to the U_LO driver schematics found on page 2 in Appendix J. The average turn-on delay from CPLD's output pin to optocoupler's output is ~214 ns ± 3 ns in both U_LO and V_HI drivers. This means, that the delay

caused by optocoupler's internal circuitry is ~180 ns, six times longer than the delay of the input driving circuitry.

Table 9. *Oscilloscope channels when measuring optocoupler's propagation delay*

Oscilloscope channel	Point of measurement	U_LO test point	Reference net
CH1	CPLD pin	TP159	GND
CH2	Optocoupler's output	TP128	LO_0V
CH3	Optocoupler's input, anode	TP6	GND
CH4	Optocoupler's input, cathode	TP242	GND
Math (CH3 – CH4)	Voltage loss of optocoupler's input	TP6 -> TP242	n/a

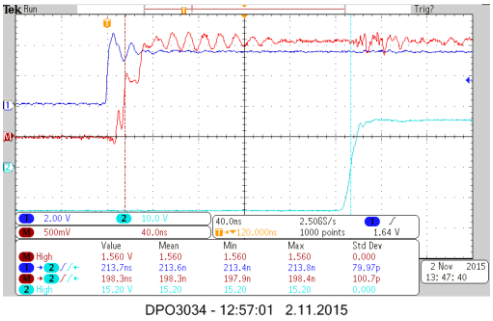

Figure 48. *Voltage waveform of CPLD pin with optocoupler's input and output in U_LO driver channel during turn-on*

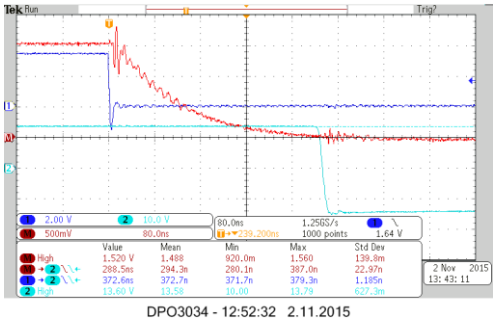

Figure 49. *Voltage waveform of CPLD pin with optocoupler's input and output in U_LO driver channel during turn-off*

The variation between different phases during turn-on seems to be around 5 ns (min vs. max delays 211,4 – 216,7 ns), which is acceptable for the presently used dead times. The largest jitter is found on V_HI phase and is ~5,3 ns of value (±3 σ). Even if the edges of signals are relatively clear and straight, this result may not be reliable. To gain more useful results, a jitter of the complete driver circuit should be observed. The standard deviation, σ, is a statistical indicator that is used for describing the deviation of the measured population, i.e. an infinitely large number of samples that represent the phenomenon. A range of ±3 σ covers 99,73 % of population. In this context, it is used to approximate the variability of the signal delays if a large number of pulses are delivered through the driver.

From the turn-off waveforms, presented in Figure 48, it can be noticed that the CPLD's output pin changes its state fast, cutting the base current from signal conversion transistor. The voltage on the optocoupler's input still remains fairly high, fed by the capacitor in parallel with it. The Math-waveform resembles a capacitor's discharge curve. Being slowly descending, the variation caused by optocoupler's internal circuit's thresholds increases. Total average delay is now 371,7 ± 8 ns. The variation range of delay between samples in different phases is 363,2 – 380,4 ns. Note the changed time scale, 80 ns/div.

Total delay of the driver circuit

Figures 50 and 51 represent the total turn-on and turn-off delays of the driver circuit with the oscilloscope setup of Table 10. Test points refer to schematics in Appendix J. The driver is considered to limit between optocoupler's output and the driver transistor's collector. If the delay was calculated using the gate voltage, results would be dependent of the chosen gate resistors. Measurements were done in ambient temperature of 25 °C.

Table 10. *Oscilloscope channels when measuring driver's total delay*

Oscilloscope channel	Point of measurement	U_LO test point	Reference net
CH1	CPLD pin	TP159	GND
CH2	Turn-on transistor's collector	TP124	LO_0V
CH3	+15 V	TP129	LO_0V
CH4	Pre-driver's turn-on transistor's collector	TP125	LO_0V

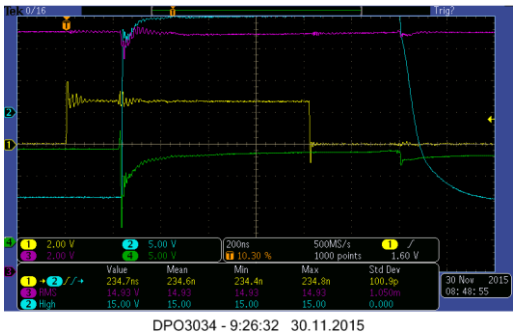

Figure 50. *Turn-on signal waveforms and delay from CPLD output to turn-on driver transistor's collector*

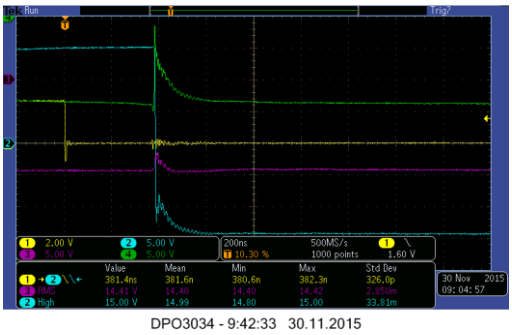

Figure 51. *Turn-off signal waveforms and delay from CPLD output to turn-off driver transistor's collector*

Turn-on delay is approximately 229 – 235 ns, which means that the delay from optocoupler's output to the gate driver transistor's collector is only around 15 ns. That makes the optocoupler as the primary cause of delay on the signal path. Total turn-off delay is around 380 – 383 ns. Since the driver's operation is symmetric, the driver's delay remains at the same level. Jitter seems to be ignorable in both cases, being < 2 ns (± 3 σ).

The corresponding delays for the reference driver were measured to be around 50 ns at turn-on and 30 ns at turn-off. The delay caused by driver circuit could be decreased by over 60 % on average by using the studied driver instead of the reference driver. However, by using a faster optocoupler, the delays and jitters could be reduced significantly more as their delays are longer. The measurement results regarding the reference driver are included in Appendix M.

4.1.4 Driver's output

In this chapter, the results of the measurements regarding the output stage capability are introduced. The output stage can be considered the most important circuit of the driver since its behavior has a significant effect on the switching of the IGBT. Together with previously measured delays, the measured values of driver's output current, voltage and their rise and fall times make the driver comparable with other drivers that may have a different internal structure.

Output current and gate voltage

Figures 52 and 53 represent the output of the driver circuit with oscilloscope setup of Table 11. The test points refer to the U_LO driver schematics found on page 2 in Appendix J. The turn-on and turn-off characteristics of output current are similar. Both have an amplitude of ~8,3 A and duration of ~600 ns.

Table 11. *Oscilloscope channels when measuring driver's output characteristics*

Oscilloscope channel	Point of measurement	U_LO test point	Reference net
CH1	Turn-on resistor's current	n/a	n/a
CH2	Turn-off resistor's current	n/a	n/a
CH3	Driver's turn-on transistor's collector	TP124	LO_0V
CH4	IGBT's gate	TP138	LO_0V

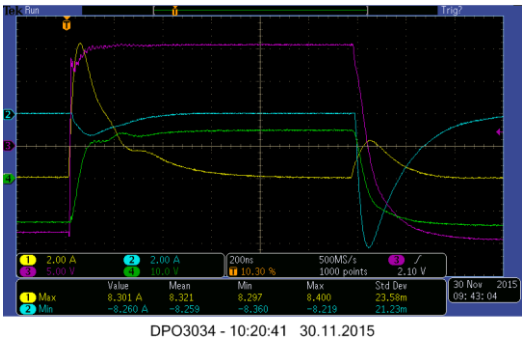

Figure 52. *Turn-on and turn-off currents, turn-on driver's collector voltage and gate voltage of U_LO during a single pulse.*

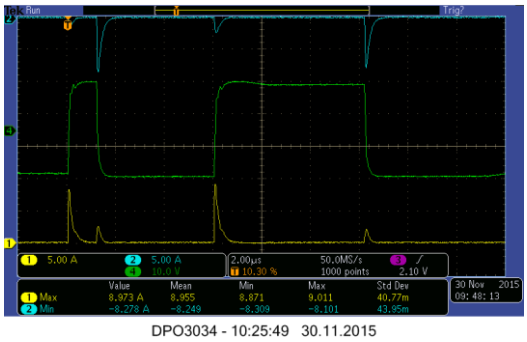

Figure 53. *Turn-on and turn-off currents and gate voltage of U_LO during two sequential pulses.*

In both turn-on and turn-off current curves there are also additional pulses during the switching, which have lower amplitude and shorter duration. As a trade-off for the capability of switching high currents, the transistors are slow to turn off. This appears as a leak of current through the push-pull stage, from +15 V supply to -15 V supply. This could be avoided by replacing the driver transistors with faster ones and adding a dead time for transition between turn-on and turn-off, but by the time of the prototyping no faster alternatives for transistors were found. The second option would mean leaving the gate floating and consciously adding delay for the switching, which is not desired.

Figure 53 visualizes the switching characteristics of the driver with two pulses with different duration. It can be noticed that a shorter pulse will cause higher waste pulses to occur. The shortest used test pulse has been chosen as ~1…1,2 us, which represents the shortest allowed pulse in company's frequency converters. Normally the pulses last longer, and therefore the 1 us pulse acts as a worst-case reference. The reason for increased waste pulse amplitude lies in the control of driver transistors. To quicken the switching for lower losses, the driver transistors are let to go closer to saturation with the kick-off circuits introduced previously. After ~2 us, the base current of push-pull stage's turn-on transistor is decreased to restore the transistor's capability to cut off current faster.

A flat phase can be seen on the turn-on current after about 300 ns from the beginning of switching process. It is caused by the Miller-capacitance of IGBT's gate and is therefore not clearly visible in the turn-off current curve. The Miller-capacitance causes the capacitance of the gate to increase during the transition from non-conductive to conductive when the gate voltage has already approached the driver's output voltage. Miller capacitance affects the switching when the IGBT module's internal chip gate voltages are ~10 V. The same applies to the turn-off event, but since the external gate pin is connected to

-15 V through a small resistance, the gate is rapidly discharged and the Miller-phenomenon is not as visible in the current graph. It can still be seen on the gate voltage on CH3, which has a gradual change in slope between 12…10 V.

The gate voltage and driver's output voltage curves of the studied driver are collected in Figures 54 and 55 together with the corresponding curves of the reference driver. Driver's output voltages are measured in between the turn-on transistor and gate resistor. The studied driver (*GST driver*) is able to provide a steady gate and output voltages that rise steeply in the beginning of switching. The output of the reference driver is prone to oscillation and the voltage transient on the gate is slower. Notable detail on the reference driver's turn-on curves is that the voltages actually seem to exceed the positive supply voltage. This kind of oscillation may be harmful if the IGBT's internal gate voltages fluctuates and causes the IGBT to switch unexpectedly. The behavior cannot be seen in the turn-off curve, decreasing the possibility of it being caused by measurement error. Oscillation may be caused by poor routing of gate traces and power supply connections.

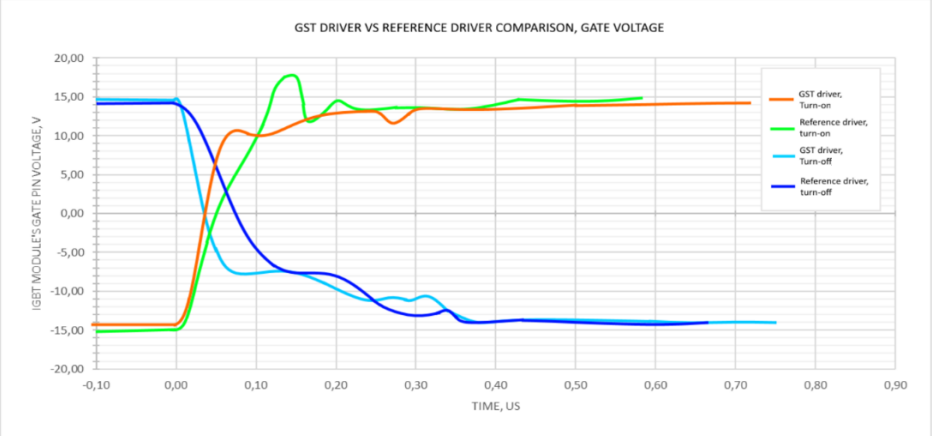

Figure 54. *Gate voltage and driver's output voltage comparison between studied driver and reference driver at turn-on.*

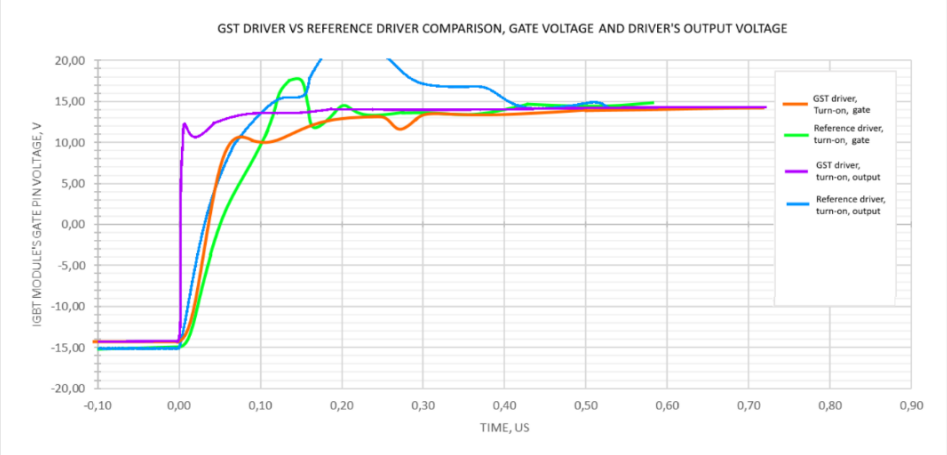

Figure 55. *Gate voltage comparison between the studied driver and reference driver at turn-on and turn-off*

The difference on the gate voltages is not clear, however. To highlight the advantages of the studied driver, the driven IGBT should be significantly larger. The 5 Ohms internal gate resistor limits the gate current, which decreases the stress of the driver circuit. As the reference driver is designed modules like the one used in the test setup, it was expected to drive them well. The reference driver also benefits from its higher steady-state gate voltage that it can offer due to missing desaturation circuit. The transistors of the reference driver are slightly closer to saturation than on the studied driver circuit, causing a lower voltage drop over them.

When focusing on the output voltages, the superiority of the studied driver is clear. Since the behavior of gate voltage is mainly defined by gate resistors, the appreciation of a driver's performance should be done according to its output voltage instead. The studied driver reaches significantly higher rate of change during switching, thus offering better adjustability than the reference driver. Also the measured gate currents are remarkably higher, being close to 7 A while the reference driver is providing only 4,5 A.

Auxiliary gate capacitor variation

In Figures 56 – 58 IGBT is driven with four different external gate capacitors setups: 0 nF, 10 nF (nominal), 22 nF and 39 nF. Unless otherwise stated, 10 nF external gate capacitor is used in all other measurements. Note that during these measurements the push-pull stage of the driver circuit had not yet been adjusted, causing the driver transistors to saturate. Therefore the absolute values of currents should not be compared with results of other chapters. The mutual ratio of the currents and losses is still applicable for the adjusted driver.

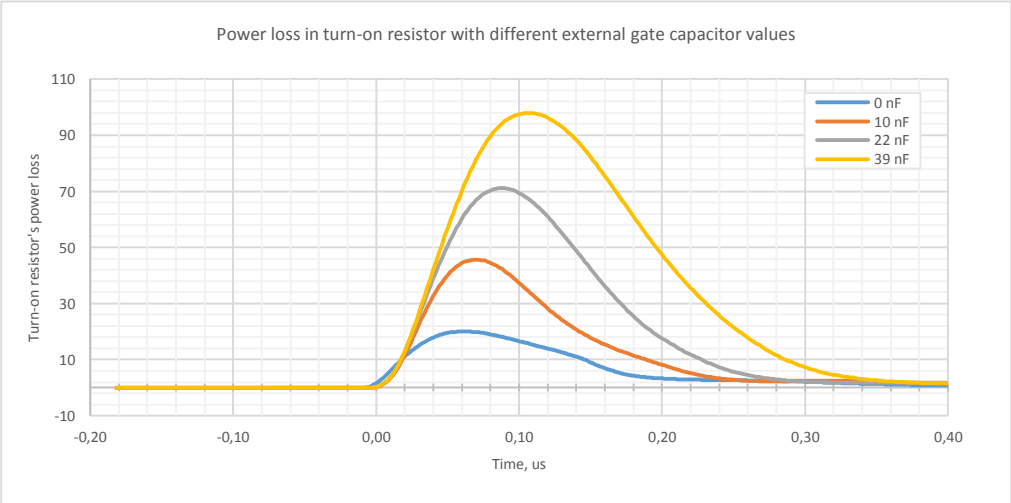

Figure 56. *Power loss in turn-on resistor with different auxiliary gate capacitor values*

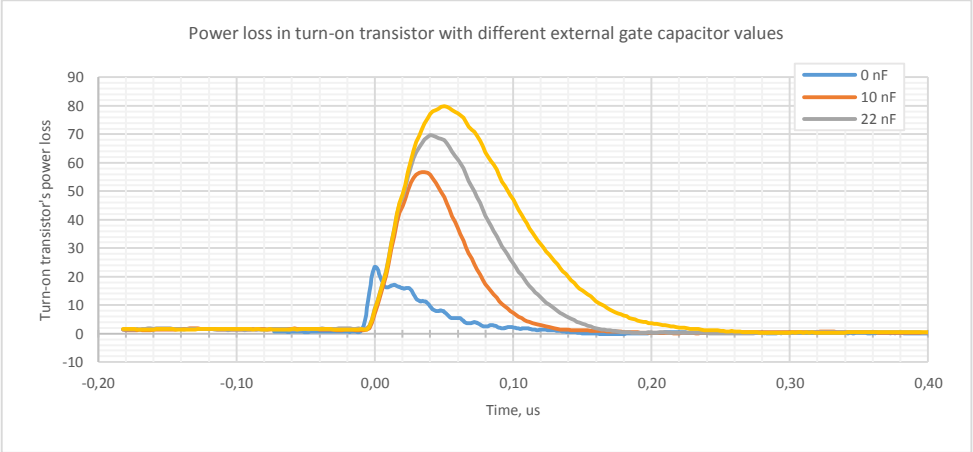

Figure 57. *Power loss in turn-on transistor with different auxiliary gate capacitor values*

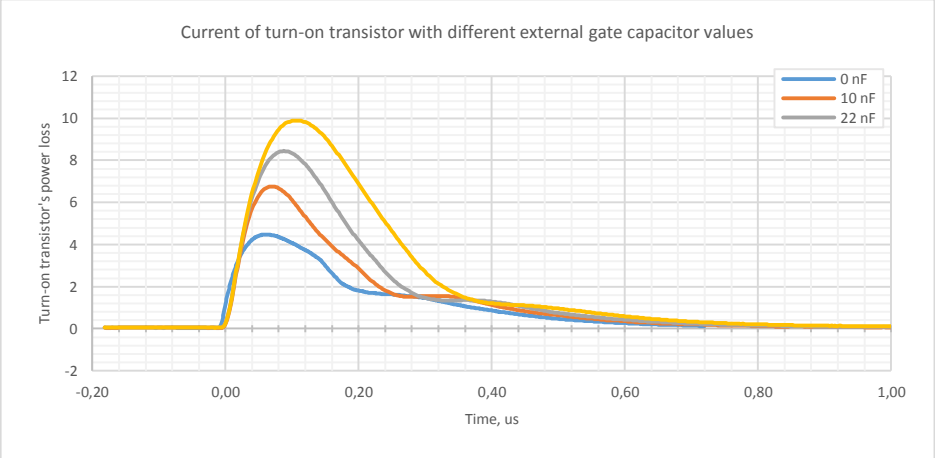

Figure 58. *Turn-on transistor's collector current with different auxiliary gate capacitor values*

Using larger auxiliary gate capacitor value the driver's output current is increased significantly due to the higher output current. Even if the IGBT's gate capacitance actually dominates in capacitance, it is still decoupled from the driver by the internal 5 Ohm gate resistor. Therefore also its effect to the current level is smaller than the auxiliary gate capacitor's. Larger capacitor was tested in the prototype to verify the current supplying capability of the driver. As can be noticed on Figure 58, the driver's output current shows no limiting at 10 A level. The output could have been stressed further by using even higher capacitances.

Also the internal gate capacitance can be verified to be close to the 36 nF specified in the datasheet [20]. When the driver's power losses of Table 12 with a 0 nF auxiliary gate capacitor and a 39 nF auxiliary gate capacitor are compared, it can be noticed that the energy taken from the +15 V supply and delivered through the driver's turn-on transistor

is almost doubled. The energy is lost in gate resistors, both internal and external. The leakage current through gate and losses of capacitors can be neglected.

The energy needed for one turn-on event is ~19 uJ, when a 10 nF auxiliary gate capacitor is assembled. With a switching frequency of 8 kHz, total power consumption of turn-on resistors is ~150 mW. Peak current through them is ~6,8 A, which causes peak power loss to be ~46 W. As the supply voltages are +/– 15 V and both gate resistors are 1 Ohm, the turn-off power consumption will be equal.

Table 12. *Effect of auxiliary gate capacitor value to the power consumption of the driver's output stage at 8 kHz switching frequency*

Auxiliary gate capacitor value	From +15 V, mW	Power loss in turn-on resistor, mW	Power loss in turn-on transistor, mW
0 nF	130,4	23,5	9,4
10 nF	182,1	45,6	31,4
22 nF	230,9	77,7	47,4
39 nF	304,0	128,4	67,5

Using different IGBT module and gate capacitor will affect the needed power, as will the used turn-on and turn-off resistors. Both positive and negative supply should be designed to provide equal power for gate drivers. If a common low side gate power is used, it should be capable of providing as many times the power needed for one gate driver as there are drivers supplied by it.

4.1.5 Thermal behavior

Since several diodes and bipolar junction transistors are used for critical tasks in the circuit, it needs to be verified that operating in high-temperature environment does not change the operation significantly or cause instability. The prototype board was inserted in an ambience testing cabin with controllable temperature. The temperature was set as 85 °C and the board was let to heat up thoroughly. After ~1 hour the temperature was considered to be stable and double pulse tests were performed for the board. The results of turn-on and turn-off behavior of the driver without active main circuit are presented in Figures H.1 and H.2 in Appendix H. The behavior of optocoupler in a high temperature environment is further discussed in Appendix G.

As Figures H.1 and H.2 depict, the driver operates correctly also in high-temperature ambience. No significant changes can be observed when comparing to the corresponding

curves in Figure 52. The peak value of the current through turn-on resistors is ~7,6 A during turn-on event. This is slightly lower when compared to the ~8,3 A measured at room temperature. Waste peak in current waveform remains approximately on the same level.

The delays show no remarkable shift from the expected values either. Since the optocoupler is the main source of delay, its behavior has the largest effect on the final value. Measured from the rising of the CPLD pin's voltage to the rising of the turn-on driver transistor's collector voltage, the turn-on delay is ~252 ns. For turn-off event the corresponding signals are falling and the delay is ~535 ns. Jitter remains at a low level in both events. Time interval has been calculated between crossings of the 50 % of the final value. In room temperature, the turn-on delay was measured to be 230…235 ns and turn-off delay ~380 ns. The main reason for the slowed operation is the increased propagation delay of the optocoupler. Figure 59 visualizes the dependency between operating temperature and propagation delays when switching the output from a high to a low level (T_{PHL}) and from a low to a high level (T_{PLH}).

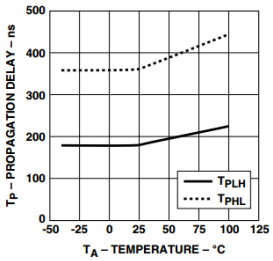

Figure 59. *The propagation delay of HCPL-J314 optocoupler in function of ambient temperature. [2]*

The behavior of optocoupler in high temperature ambience was also measured individually. Results can be seen in Appendix G. The measurement was performed using V_HI driver. The optocoupler in V_HI driver circuitry had to be replaced due to failure caused by a wrong grounding point of oscilloscope's probe. This means that the results are not completely comparable with the previous measurements.

Increased delays in high ambient temperatures should be taken into account when defining the allowed minimum pulse lengths and dead times for a frequency converter to avoid short cross conductions. Optocoupler's datasheet advises that a maximum propagation delay of 500 ns should be used to avoid overlapping in IGBT control signals. This means having a maximum dead time of 1 us. [2] In addition to this, it should be taken into account that push-pull stage transistors have a relatively long turn-off time, which may cause a need for using even longer dead times. The gain of pre-driver and driver transistors increase with temperature [21]. The effect is not significant for the pre-driver which operates as a current sink and is therefore naturally restricted from output current increase.

Desaturation circuitry prevent push-pull stage transistors from entering saturation. By using two diodes in series in the desaturation circuitry, there is an increased margin for decreasing of the diodes' forward voltages due to increased temperature. In the measured temperatures, the push-pull stage transistors did not enter saturation, which means that desaturation circuitry works well in the given temperature range.

Also the local heat generation of the driver was verified at normal room temperature. The power loss in the driver transistors consists of the loss caused by the base current and the collector current. The collector current includes both the gate current and the waste current that is conducted straight through the push-pull stage. The simulations estimate the power loss to be between 200…300 mW at a 50 % duty cycle. The FZT851 and FZT951 transistors are only available in SOT223 SMD package which is capable of handling up to 3 W of power with a large heatsinking pad. With a reasonably sized heatsinking pad, the power loss can be ~1 W. The heating of the push-pull transistors V33 and V34 was tested by applying a continuous 10 kHz driving signal to the driver's input and letting the temperature to steady for ~2 hours at a room temperature of 25 °C. The heating of the board was then measured with a thermal imager Fluke Ti10. The image obtained from the thermal camera can be found in Figure 60.

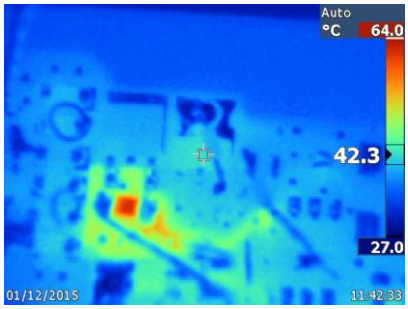

Figure 60. *Thermal image of the driver circuit*

The temperature rise of V33 and V34 was measured to be ~17 °C. The highest heat spot in the image is the pre-driver's current generator resistor R90, which has a temperature difference of ~40 °C. Dividing the heat load for two separate components is advised.

4.2 Main circuit

This chapter introduces the switching behavior of the main circuit when the IGBT is switched in normal operating conditions with the prototype driver. Appraising the results includes outlining the critical characteristics of both the datasheet of the driven IGBT module and a reference driver circuit that was tested by driving a similar IGBT module.

4.2.1 The effect of a high-voltage main circuit to the driver

Since the previous measurements were performed without a voltage on the DC-link, it needed to be verified that a high voltage over the IGBT would not affect the operation of the driver. The verification was done by comparing the waveforms of the driver with and without voltage on the main circuit. The waveforms of the driver at 85 °C ambient temperature but without voltage in the DC-link are included in Appendix H. The IGBT's gate pin voltage reaches the level of 12 V in ~70 ns after it has begun to ascend. Reaching 95 % of the final voltage takes around 300 ns. During turn-off descending from 14 V to 0 V takes about 50 ns and reaching 95 % of the final voltage between 300 and 400 ns.

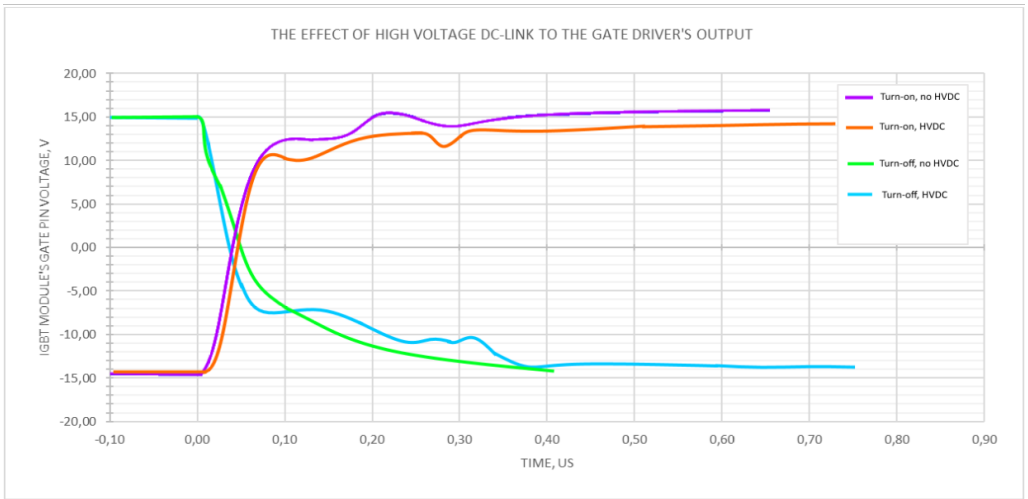

Figure 61. *The effect of high voltage DC-link to the gate voltage during switching*

A voltage of 600 V_{DC} was applied in the main circuit in the measurements of Appendix D. When the behavior of gate pin voltage is observed in Figures D.2 and D.6, it can be seen that the knee-point of gate voltage curve during turn-on has slightly decreased to around 10 V from the situation of Figures H.1 and H.2. It is, however, reached in less than 50 ns. After that increasing is slower and reaching 95 % of the final voltage takes around 400 ns. The reason for the extended period is the charging of Miller capacitance. The difference between the two stages of gate switching has now become better visible also during turn-off. Again, the reason is the Miller capacitance, which is now slowly charged through the IGBT module's large internal gate resistor. The gate voltage curves for turn-on and turn-off are collected in Figure 61. Although the difference between the results is visible, it is limited to the gate voltage and current. The waveform of driver's turn-on transistor's collector voltage keeps its shape as can be verified from Figure C.4 in Appendix C. Also the differences in the gate voltage and current waveforms are relatively small. Therefore the results done for the rest of the driver circuit were considered reliable.

4.2.2 Found issues

While the IGBT losses were measured, it became clear that the high- and low-side IGBT's did not produce similar losses and waveforms for collector current and collector-emitter voltage. With the same driver assembly, low-side switches were producing over twice as high switching losses as the high-side switches. After testing with different driver channels and IGBT modules, it was found out that the reason for this was the negative feedback for gate voltage in high collector current transients, caused by the stray inductance of the bond wires.

High-side switches operate as expected due to the proper Kelvin emitters that are used for gate voltage reference and connected directly to the IGBT chip. More detailed explanation of the behavior is included in the Appendix C. For this reason, only high-side switch was used for measurements of losses, GST operation and final main circuit waveforms.

4.2.3 Switching delay

The switching delays in this scope are defined as the times from the switching of optocoupler's output to the moment when the IGBT's switching is considered to be ended. This highlights the performance of the driver – IGBT -combination. The measurements were conducted with a 150 A load current at 25 °C ambient temperature for both turn-on and turn-off by using V_HI driver. The results are combined in Table 13.

Table 13. *Switching delay comparison between the studied prototype and the reference design*

Driver	Turn-on switching delay, ns	Turn-off switching delay, ns
70CVB01979A prototype	335	360
Reference driver	325	525

As can be seen from the results, the difference in turn-on switching delays is insignificant. This is caused by the higher steady-state gate voltage of the reference driver. Lower gate voltage extends the switching of the studied driver, thus affecting the total delay. If higher power supply voltages were used, the studied driver would presumably achieve shorter delay.

4.2.4 Switching waveforms and thermal behavior

The main circuit waveforms for switching of V_HI IGBT are included in Appendix D. The measurements were ran at three different IGBT module temperatures: 25 °C, 85 °C

and 150 °C. In all measurements, a DC-link voltage of 600 V and nominal collector current of 150 A were used. Additionally, one test was performed with a 900 V DC-link voltage and 150 A collector current. Both turn-on and turn-off waveforms were captured and the results are collected in Table 14. The dI_C/dt is calculated to the primary change, not for the whole switching period. The dV/dt, however, was calculated for the whole switching period at turn-on since it keeps changing throughout the switching process. The momentary maximum value for dV/dt is therefore higher at some points of the curve. For turn-off, it was calculated for the primary slope as was the dI_C/dt.

Table 14. *Key values measured at switching with different IGBT temperatures*

Variable	Turn-on at 25 °C	Turn-on at 150 °C	Turn-off at 25 °C	Turn-off at 150 °C	Turn-on at 25 °C	Turn-off at 25 °C
DC-link voltage, [V]	600	600	600	600	900	900
Switching time, [ns]	186	259	215	383	236	173
FWD recovery current peak, [A]	250	285	-	-	267	-
FWD recovery peak duration, [ns]	60	80	-	-	60	-
dV_{CE}/dt, [kV/us]	-3,2	-2,3	4,6	4,2	-3,8	7,2
dI_C/dt, [kA/us]	5,5	4,7	-1,2	-0,6	6,6	3,1
Switching loss, [mJ]	9,7	15,5	7,5	13,7	18,7	9,8
Turn-off overshoot, [V]	-	-	65	20	-	45

The resulted waveforms represent relatively well the typical waveforms introduced earlier in the theory. The Miller plateau is well noticeable in the V_{CE} curves of turn-on switching. During turn-off switching, the V_{CE} can be seen to almost reach its DC-link value before the collector current starts decreasing. The current tailing and free-wheeling diode's reverse recovery current peak are visible, too.

The most significant effect of higher operating temperature for IGBT's turn-on can be seen clearly as longer falling time of V_{CE}. The Miller plateau is wider and located at higher voltage level. As the plateau is located close to the level of 480 V and lasts for about 50 ns at 25 °C, it ascends to the level of 490 V and lasts close to 70 ns at 150 °C. The switching time is also significantly longer at the higher temperature, causing the losses to increase. Besides increased losses, the slower switching has some advantages,

too. The commutation is smoother at the higher temperature, which can be seen as the oscillation or dip in the collector current during turn-on is flattened at 150 °C. At 25 °C it is clearly visible. The same applies for turn-off, as the turn-off overshoot amplitude is decreased at high chip temperatures.

The typical switching times declared by the datasheet at the nominal operating point at 150 °C with 1 Ohm gate resistors are 350 ns for turn-off, 110 ns for turn-on. As the turn-off switching time is close to the value given in the datasheet, the turn-on delay is significantly higher. This, however, can be explained by the highly non-linear behavior of the IGBT at the linear region. If the IGBT module's manufacturer has measured the delays using +/– 15 V gate voltages without taking into account the voltage drop on the driver transistors, the time will be shorter. For turn-off, the effect is smaller as discussed earlier.

The measured reverse recovery peak currents are significantly lower than the nominal values stated in the datasheet. At 150 °C and 4,7 kA/us the peak value should be around 180…185 A, which is additional to the base level of 150 A load current. [20] The corresponding measured peak value is only 135 A. The difference may be explained by different methods of calculating the dI_C/dt value.

When comparing the effect of increasing DC-link voltage from 600 V_{DC} to 900 V_{DC}, as done in Figures D.1 and D.4, as well as in Figures D.5 and D.8 in Appendix D, the most significant variable seems to be the high rates of change, i.e. dV_{CE}/dt and dI_C/dt. In all ways, using 900 V DC-link voltage stresses the switching components and the load motor more. For the driver circuit, however, handling the high DC-link voltages seem not to be a problem. The driver still operates as expected.

4.2.5 Losses

The results from IGBT's switching energy measurements are included in Appendix D and collected in Table 14. As a comparison, the datasheet declares the typical turn-on energy at the nominal load of 150 A, at 150 °C IGBT temperature and using 1 Ohm gate resistors to be 9 mJ for turn-on, 15,5 mJ for turn-off and 11 mJ for the reverse recovery. [20]

When compared to the values given in the datasheet, the measured turn-off energy can be noticed to be lower than the declared nominal value. The measured turn-on energy, however, is around 70 % higher than expected. But as the losses are highly dependent on the value of the gate-emitter voltage, the used 14…14,5 V gate voltage can cause this difference. If an alternative +17 V / –10 V gate power supply was used, the losses would be significantly lower.

As already mentioned earlier, it was noticed during measurements that the losses were differing between high- and low-side switches. The reason for this was a difference in the gate contacts inside the IGBT module. Since the structure of high-side IGBT is more commonly used, only V_HI driver and IGBT was used in the final main circuit measurements. The results from measurements performed with U_LO IGBT were not comparable with the datasheet values due to their high level of losses. The topic is further discussed in Appendix C.

The results from switching energy measurement done for the reference driver at 25 °C with 150 A load current and 600 V DC-link voltage can be found from Appendix M. The turn-on energy was measured as 7,9 mJ and turn-off energy as 9,7 mJ. The total switching loss for one cycle is 2 % higher than with the studied driver, which can be regarded insignificant. The reason for the reference driver's good performance is again the unexpectedly high gate voltages and the fact that the benefits of the studied driver are not visible when driving small-scale IGBT modules with high internal gate resistor value.

4.3 Soft turn-off circuit

The GST functionality is tested with 70CVB01979A by simulating an over current detection with a timed action on CPLD. The response for an over current detection on CPLD is stopping normal modulation immediately and setting the GST output pin to a logical high level for a predetermined period of time.

4.3.1 Soft turn-off resistor variation

As the turn-off overshoot amplitude is dependent of the main circuit structure, it had to be solved first, which values are optimal for the soft turn-off resistor and capacitor. The results gained with different values of R_{GST} are included in Appendix E. The combined curves are introduced in Figures 62-64. The curves are drawn as moving averages of 10 sequential data points. The trigger event in the oscilloscope was set as the decrease of the gate voltage. The trigger settings were the same for all curves. This clarifies the difference in the IGBT's switching behavior after turn-off had been started, because the delays between different graphs are now comparable. In these situations, the soft turn-off capacitor, C_{GST}, has been 10 nF. The curves representing a normal turn-off are also included as reference.

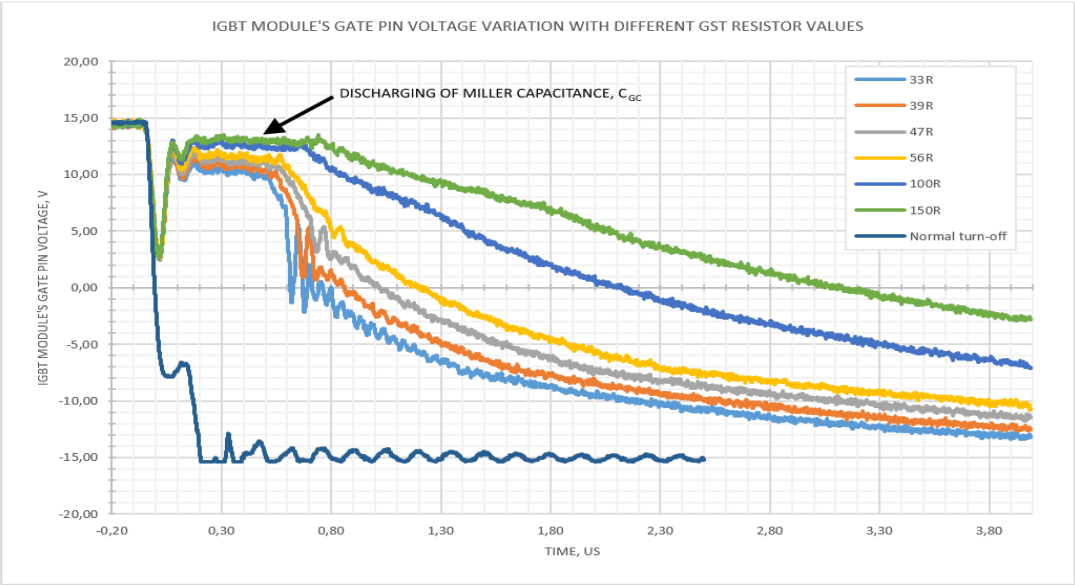

Figure 62. *Decrease of gate pin voltage with different R_{GST} values*

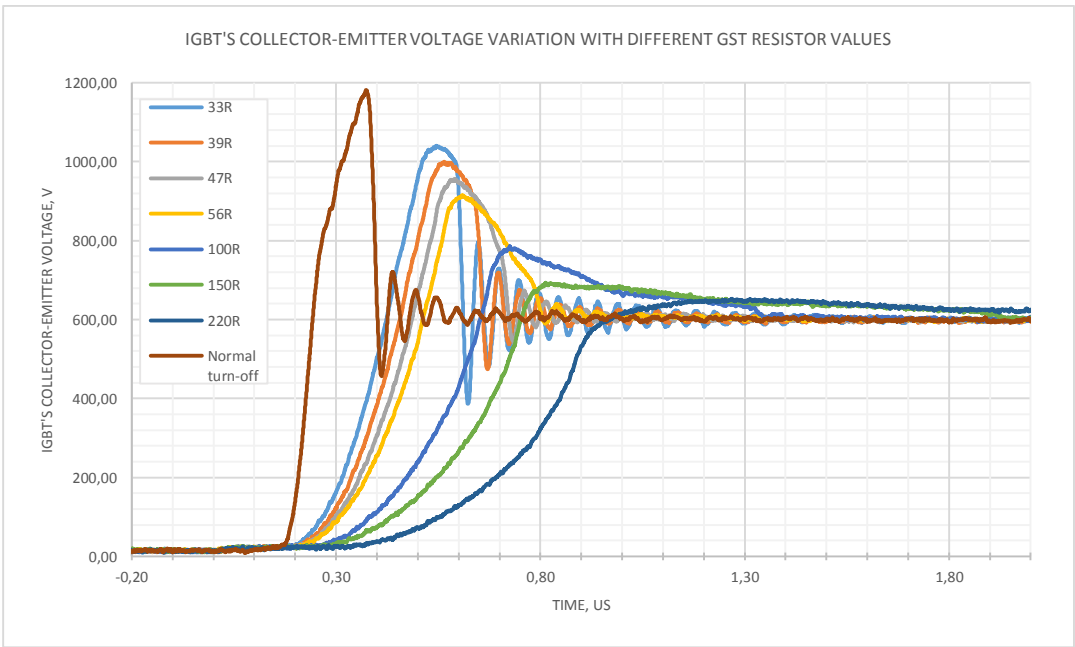

Figure 63. *Turn-off overshoots with different R_{GST} values*

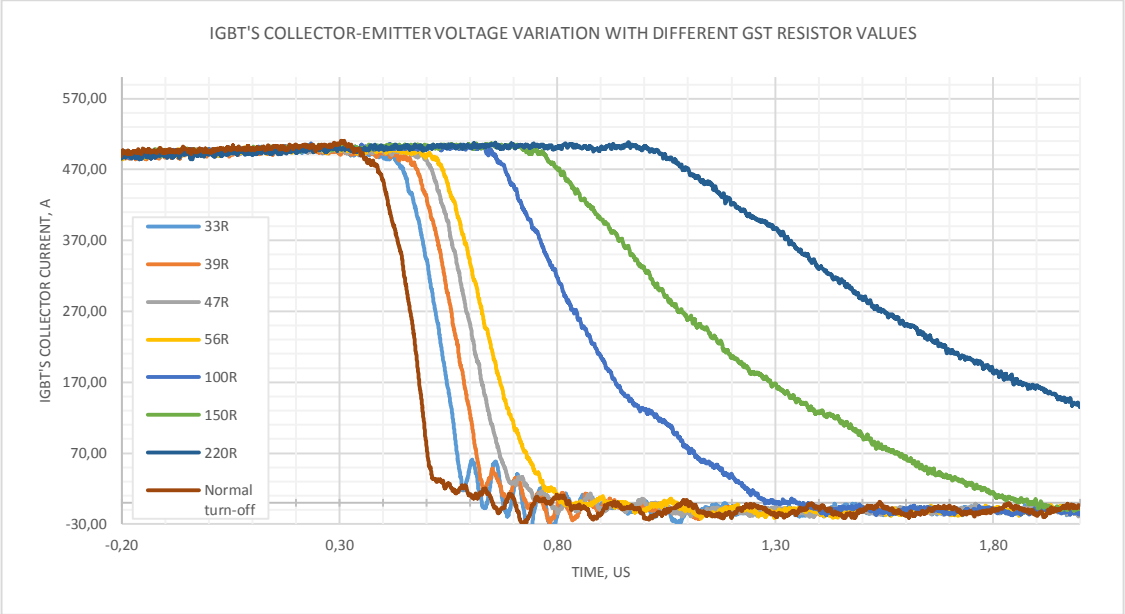

Figure 64. *Decrease of IGBT's collector current with different R_{GST} values*

The first effect of soft turn-off can be seen in Figure 62. The higher the resistance of the discharging resistor is, the longer time the discharging of gate capacitances will take. The downwards peak in the beginning of the gate discharging process is caused by two factors: the momentary activation of the driver's normal turn-off and the charging of soft turn-off capacitor, C_{GST}. Since the gate charge dominates the capacitance of auxiliary gate capacitor, the gate voltage is recovered to the level of 10…13 V after the negative boosting has ended. After that the gate is discharged through the R_{GST}. The purpose for this negative boosting is to take the IGBT immediately to the linear region to save time and to prevent the short circuit current from increasing further.

Figure 63 presents the desired effect of the soft turn-off – the decreased turn-off overshoot voltages when a high current short circuit on the output phase is switched off. By increasing the R_{GST} value, the overshoot amplitude can be limited. Simultaneously the ringing is dampened due to lower current and voltage transients in the main circuit. The downside in using high resistance value for R_{GST} can be seen in Figure 64, as the short circuit current will stay present longer and the circuit becomes more sensitive to the value of the parallel soft turn-off capacitor, C_{GST}, value.

4.3.2 Soft turn-off capacitor variation

The oscilloscope screen captures gained with different values of C_{GST} are included in Appendix E in Figures E.4, E.7 and E.8. The combined curves are introduced in Figures 65-66. The curves are drawn according to the oscilloscope screen captures. The initial moment was adjusted for redrawn images to match with the starting moment of soft turn-

off. The delays between different graphs are therefore comparable. The soft turn-off resistor, R_{GST}, has been 100 Ω in all the following measurements.

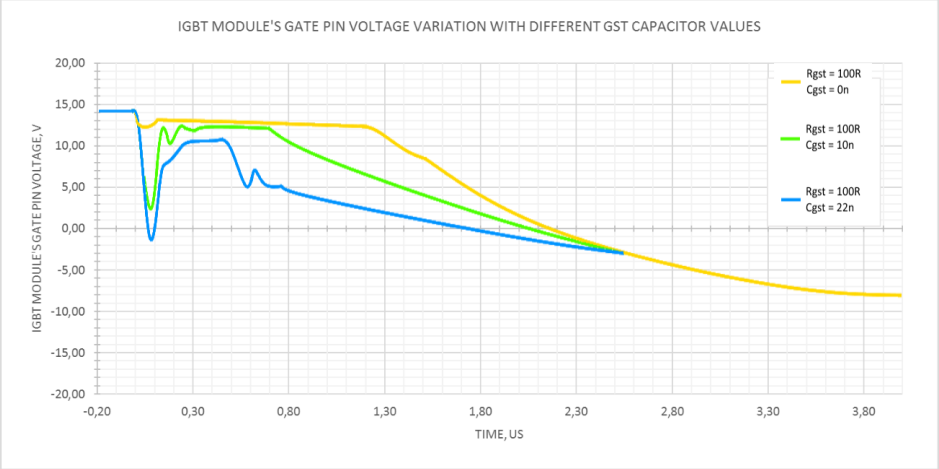

Figure 65. *Decrease of gate pin voltage with different R_{GST} values*

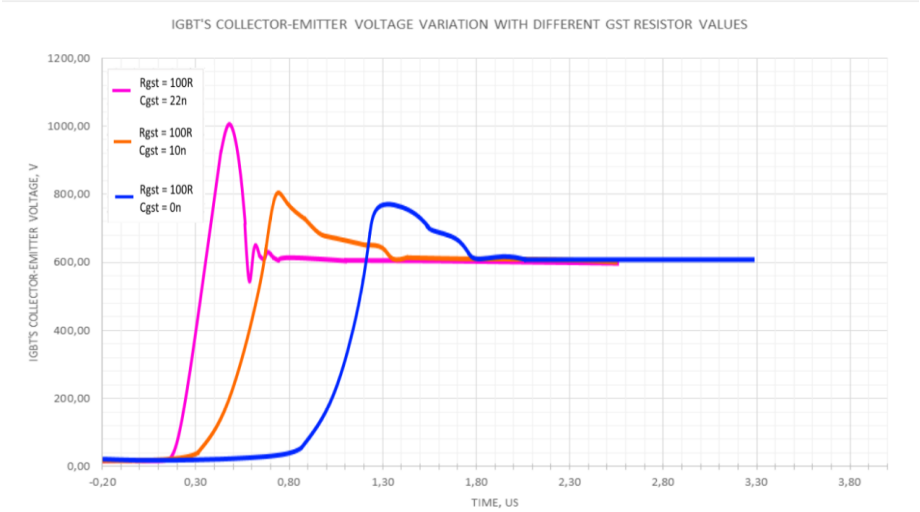

Figure 66. *Turn-off overshoots with different R_{GST} values*

The capacitor C_{GST} (C106 on V_HI) causes a capacitive voltage divider to form on the gate circuit immediately after the activation of soft turn-off and part of the gate charge is ejected from the gate's parasitic capacitances and the auxiliary gate capacitor. The voltage dip is steep due to the relatively small auxiliary gate capacitor, but after the C_{GST} is charged, the gate voltage recovers to a level that is defined by the residual charge on the gate's parasitic capacitances. As already discussed, the parasitic gate capacitances are separated from the gate pin by the internal gate resistors, creating a low-pass filter on the gate.

Since the discharging through the soft turn-off resistor takes relatively long time, the capacitance of C_{GST} should be adjusted correctly to a value that is large enough for bringing

the IGBT to the linear region. If a too large capacitance is used, the IGBT traverses through the linear region fast, thus causing high overshoot amplitudes to occur. Too low capacitance, on the other hand, may cause the short circuit to stay present for an extended period of time. Figures 65 and 66 introduce examples of both situations. When no C_{GST} is assembled (0 nF), discharging of Miller capacitance takes significantly longer than when using a 10 nF capacitor. On the other hand, using 22 nF capacitor causes too large charge to be ejected from the gate. This increases the turn-off overshoot voltage. After the voltage over CGST is stabilized, the gate discharging current will be conducted through the soft turn-off resistor R106. This causes the tails of the gate voltage curves to resemble a capacitor's discharging curve. 10 nF was considered as an optimal value for C_{GST}, since it speeds up the turn-off process without increasing the turn-off overshoot voltage significantly. The value depends on the used IGBT module and the value of auxiliary gate capacitor and should therefore be adjusted for each setup individually.

4.3.3 Final soft turn-off circuit

The final values of the R_{GST} and C_{GST} were chosen as 150 Ohms and 10 nF to make a compromise between the caused delay and the turn-off overshoot amplitude. The system was tested by turning off a current of 520 A and 900 A with a DC-link voltage that was varied between 600 V to 800 V. The tests were performed without heating the IGBTs. The results with 900 A load current and varied DC-link voltage are included in Appendix F. Also Figure E.5 in Appendix E represents the operation of GST circuit with the final assembly with load current of 520 A and DC-link voltage of 600 V, while Figure E.1 acts as a reference of normal turn-off at the same operating point.

Figure F.1 represents the reference cut-off, done by using normal turn-off resistor and 600 V DC-link voltage. The overshoot is harsh, and it is followed by severe ringing in the V_{CE} curve. In Figures F.2 and F.3, the DC-link voltage has been increased first to 700 V and then to 800 V. The cut-offs have been done by GST. Since the pulse widths were maintained the same, the switched current level is slightly higher than in the reference measurement. These tests were done to prove that by using the soft turn-off, the same IGBT modules could be used in converters with higher DC-link voltage without increasing the risk of IGBT failure caused by overvoltage. This would lower the costs and enhance the energy efficiency due to lower conduction losses of IGBT modules with lower voltage rating. The results are promising: the overshoot voltages stay well under specified maximum levels even if the current can be regarded ample for this kind of assembly. It was also noticed that the overshoot actually seems to follow the dependency defined in Formulas 5 and 6 in the theory part. If the overshoot amplitudes are divided by the rates of change measured for the collector current in Figures F.1 – F.3, the result seems to vary between the range of 120…150 V/A/µs. That can be regarded as a main circuit layout specific constant.

When a soft turn-off is performed with 600 $V_{DC\text{-}link}$, load current of 520 A and with the final circuit assembly, the turn-off voltage overshoots were reduced by 82 % when compared to the overshoots caused by normal turn-off. Figures E.1 and E.5 in Appendix E represent the compared turn-offs. Turn-off voltage overshoot, V_{TO}, was defined as a difference of measured maximum voltage during turn-off and the DC-link voltage. The decrease is therefore:

$$\Delta V_{TO}(\%) = \left(1 - \frac{V_{TO,GST}}{V_{TO,NORMAL\ TURN-OFF}}\right) * 100\ \%$$

$$= \left(1 - \frac{704\ V - 600\ V}{1192\ V - 600\ V}\right) * 100\ \% = 82{,}4\ \%$$

Even though the current in this measurement is lower, the observed behavior can generalized to cover the behavior of the switching circuit at all operating points: the overshoot voltages can be significantly lowered by using soft turn-off.

In the end of the measurements, the current and DC-link voltage were gradually increased while normal and GST turn-offs were executed sequentially. The aim was to solve the withstanding limits for the IGBT module with normal turn-off. It would have simultaneously been proven that by using the GST turn-off, the module would have sustained operational due to lower voltage stress. This test, however, was not succeeded due to the limiting of collector current as a result of significantly increased collector current. At this point, the IGBT module had already survived V_{CE} voltage peaks exceeding its specified withstanding limits.

The R_{GST} and C_{GST} values in the soft turn-off circuit setup are module-specific and should always be verified by testing with a couple of resistor and capacitor values. It is advisable to first select the resistance, since in a properly adjusted GST circuit it is defining the overshoot level. Capacitor is mainly used for compensating the delay that is caused by the longer discharging time before the IGBT enters the linear region.

5. CONCLUSION

This thesis research consisted of developing a new gate driver for controlling an IGBT switch used for frequency converters. Although the final focus and outcome of the thesis changed from the originally intended soft turn-off circuitry towards the driver circuit itself, the basic structure maintained the same. The work included a wide scale of design phases from simulations to interpreting the measurement results, albeit the final implementation to a fully working device had to be left out of scope due to limited time resources. As an output from the research, a fully verified and documented gate driver was brought to the company's design library.

The developed gate driver proved to be capable for fast high current switching. The gate current indicated no damping at a value of 7 A. With a larger IGBT module the peak gate current values are likely to reach levels close to 13 A, limited by the maximum value of the driver's output stage transistors and the waste pulse conducted through the output stage. The gate currents are high enough for switching high-current IGBTs used in large converters. The turn-on and turn-off delays between the optocoupler and the driver's output were decreased to ~15 ns, which is a level that can be considered very low for the studied topology. Further reduction of delays is more likely to be done by changing the type of the optocoupler. The same applies for the jitter; the jitter levels on the driver are low mainly due to the short total delays. The jitter and the temperature-related change of delay of the optocoupler are significant when compared to the driver.

The main disadvantage of the driver is its large number of components that causes increase in component cost and in the need for PCB area. On the other hand, most of the components are relatively small and low-cost. Second drawback is the driver's power consumption which can be considered high when compared to drivers based on MOSFETs.

When compared to the reference gate driver, the developed driver achieved significantly better performance in terms of delays, gate currents, and rise and fall times. The reference driver performed better with the IGBT's turn-on switching loss, which is mainly caused by its slightly higher gate voltage. Other results were close to equal. The key values are collected in Table 15. The turn-off losses and delays of the developed driver could be significantly decreased by using higher gate supply voltages. The developed driver would also perform better in comparison if a larger IGBT module was used.

Table 15. *Comparison of key performance values between the developed gate driver and a reference gate driver*

Variable	New driver with soft turn-off	Reference driver
Gate voltage levels, [V]	±14,4 V	±14,6 V
Output voltage rise/fall time, -14 V to 12 V, [ns]	10	90
Driver's delay, turn-on (excl. optocoupler), [ns]	15	30
Driver's delay, turn-off (excl. optocoupler), [ns]	15	50
Peak current to gate with 1 R gate resistor, [A]	6,8	4,5
Continuous power consumption, [mW]	~600	Not measured
IGBT switching delay, turn-on, [ns]	335	325
IGBT switching delay, turn-off, [ns]	360	525
IGBT switching loss, turn-on, [mJ]	9,7	7,9
IGBT switching loss, turn-off, [mJ]	7,5	9,7
Operational component count, [pcs]	24	9
Driver stage transistors	BJT, +20/-15 A	BJT, ±16 A
Soft turn-off	Optional	Not available
Desaturation circuit for driver transistors	Yes	Not available

Also the developed soft turn-off circuit was considered very effective. By using soft turn-off for switching off a high current short circuit, the caused turn-off voltage overshoots were reduced by 82 %. This would reduce the converter failures caused by short circuits significantly if the fast rising short circuit current is recognized fast enough.

For future improvement, some components need to be changed. Most of them are over-rated for the application, but there are also some that should be replaced to gain better reliability. Transistors in the soft turn-off circuit and pre-driver are rated for 6 A peak

current and 2 W continuous power, but their true load is only a fraction of that. The resistors in the pre-driver's current sink should be assembled as MELF resistors and their continuous power consumption should be matched with the power rating. For layout considerations, attention should be paid for the routing between the driver's reference ground and the IGBT's emitter.

Before the driver is taken into commercial use, it is advised to perform further tests with a larger IGBT module. The module used in the test setup proved too small for stressing the gate driver properly. Depending on the chosen IGBT module, also using higher positive gate power supply voltage should be considered. The future development of the driver prototype continues by combining it with the fast di_C/dt protection.

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APPENDIX A: TABLE OF COMPONENT FUNCTIONS

In this appendix, the functions for individual components are listed. The listing is done for the components in U_LO driver, but as all the drivers are identical, the functions are valid also for the corresponding components in other driver channels.

FUNCTION	CONTROLLED BY	SIGNAL LEVELS / REFERENCE POINT	RELATED COMPONENTS	COMPONENT FUNCTION	NOTES
USER INTERFACE	Inputs: User Outputs: Logic on CPLD board	Keys not used: +3V3 pull-up, external resistors for better reliability Keys used: 0 V Reference: GND	S1 – S6	Provides user interface for triggering gate pulses.	Programmable. Recent setup: S1 = Start S2 = GST timer triggering S3 = Invert bridge S4 = Reset S5, S6 = Not used
			R10, R17, R36 – R40	Pull-up for key signals.	Internal pull-ups for the CPLD input pins could also be used.
			R134, C64 R135, C63 R136, C62 R137, C44 R138, C16 R139, C9	RC-filtering for key signals.	
			X9	Measurement connector for observing the gate driving signals (CPLD board's output)	
DI/DT TRIGGER BOARD INTERFACE	Inputs: Di/dt trigger circuits in X7, such as 70CVB0201 3	Fault detected: GND Normal state: +3.3 V Reference: GND	X7	Connection to di/dt trigger board.	Pinout: 1: +3V3 2: Trigger_1 input 3: Trigger_2 input 4: GND +3V3 and Trigger_2 are optional signals
			R140, R141, C29, C30	RC-filtering for the di/dt trigger input signals.	
			R99, R100	Pull-ups for the di/dt trigger input signal lines	Internal pull-ups for the CPLD input pins could also be used.
Signal conversion circuit	CPLD board	Input: Active: +3.3 VDC Not active: 0 V Reference: GND	V9 – V11, V19 – V22, V58 R38, R41, R87, R88, R101, R108, R114, R115	Voltage to current signal transition	CPLD switches transistors on/off with +3.3 VDC. When the transistors conduct, the current is limited to ~17 mA. Otherwise current is 0 mA.
Gate driver, U_LO_G	Control board of 70CVB0197 9, connector X17	On state:17mA current sink / off state: high impedance Reference: DC-	H4	Provides functional isolation for gate drive signal	Has about 0,5A max output current for both source and sink
			R97, C20	Needed to filter differential mode noise from gate drive signal	Capacitor value should be kept as small and resistor value as large as possible for not to cause extra delay to IGBT switching
			R3, R15	Resistors are for filtering common mode noise from gate drive signal	The resistance should not be increased to maintain 17 mA current during on-state (~12 mA to optocoupler)
			C46, C75	Supply filter capacitors for optocoupler	
			R95, R45	Voltage divider for current sink/source input	Current sink/source input voltage needs to be limited between +/- 10 V to prevent steady-state saturation of V35 and V36

<table>
<tr><th>FUNCTION</th><th>CONTROLLED BY</th><th>SIGNAL LEVELS / REFERENCE POINT</th><th>RELATED COMPONENTS</th><th>COMPONENT FUNCTION</th><th>NOTES</th></tr>
<tr><td></td><td></td><td></td><td>C22</td><td>"Kick-off" capacitor for predriver's input</td><td>C22 is used to allow V35 and V36 to shortly enter to saturation after switching. This makes the transition time in gate voltage shorter.</td></tr>
<tr><td></td><td></td><td></td><td>V35, V36, R50, R90</td><td>Pre-driver current generator</td><td>The resistors limit the predriver's current in continuous state to ~50 mA</td></tr>
<tr><td></td><td></td><td></td><td>C36</td><td>"Kick-off" capacitor for predriver</td><td>C36 is used to allow V35 and V36 to pass a peak of higher current after switching. This makes the transition time in gate voltage shorter. The peak lasts ~1,5 us, after which the current is stabilized to around 55 mA. Current peak causes the driver transistors V33 and V34 to shortly enter into saturation, providing higher gate current during switching.</td></tr>
<tr><td></td><td></td><td></td><td>V29</td><td>Through-conduction prevention for predriver</td><td>Forward voltages of V29 ensure a state with ~0 VDC optocoupler output where neither V35 nor V36 is conducting. Without V29, a high-current pulse would run through current generator during the switching of optocoupler.</td></tr>
<tr><td></td><td></td><td></td><td>V33, V34</td><td>Driver transistors</td><td>Driver transistors are high-current, fast recovering power transistors. Using slower transistors, there would be a high-current peak flowing from +15 V to -15V during the switching.

FZT851 (NPN) has peak pulse current of 20A, FZT951 (PNP) 15A.</td></tr>
<tr><td></td><td></td><td></td><td>R133
R122</td><td></td><td>Base-emitter resistors of push-pull driver transistors. Used to achieve faster turning off of the transistors V33 and V34. Without these resistors the turn-on and turn-off transistors were measured to be simultaneously conductive during switching.</td></tr>
<tr><td></td><td></td><td></td><td>R147
R148</td><td></td><td>Base resistors of push-pull driver transistors. Used to stabilize the behavior of the transistors during switching. Without these resistors the turn-on and turn-off transistors were measured to be simultaneously conductive during switching.</td></tr>
<tr><td></td><td></td><td></td><td>V16, V27
V14, V30</td><td>Saturation prevention for driver transistors</td><td>The forward voltages of diodes in series with driver transistor's base cause the base current to decrease, if the transistor tries to enter into saturation.

V16 forces the base of V34 to be on ~0,5 V higher potential than the collector. If the collector voltage tries to rise, part of the predriver's constant current will be drawn from collector instead of base.

The diode between V27:3 and V27:1 blocks the current from +15V to gate resistors, pass V34, during off-state.</td></tr>
<tr><td></td><td></td><td></td><td>C98-C101</td><td>Supply capacitors for push-pull driver</td><td>In test setup C46 was increased to 12 uF by adding a 10 uF capacitor in parallel to 2 uF. This was done due to weak x_0V connection on layout.</td></tr>
<tr><td></td><td></td><td></td><td>R2, R9, R96, X25

R130 – R132, X24</td><td>Gate resistors</td><td>Adjustable gate resistance for research purposes. The desired turn-on and turn-off resistances can be chosen independently by combining jumpers in connectors X24 and X25. This helps measuring the switching times and –losses of IGBTs in function of R_G. Pulse power tolerant resistors required (MELF MMB0207 used). In the used setup, parallel resistance of 1 Ohm was used.
<table>
<tr><th colspan="4">GATE RESISTOR COMBINATIONS:</th></tr>
<tr><th>2R2</th><th>4R7</th><th>12R</th><th>PARAL-</th></tr>
<tr><td>1</td><td></td><td></td><td>2,20</td></tr>
<tr><td></td><td>1</td><td></td><td>4,70</td></tr>
<tr><td></td><td></td><td>1</td><td>12,00</td></tr>
<tr><td>1</td><td>1</td><td></td><td>1,50</td></tr>
<tr><td>1</td><td></td><td>1</td><td>1,86</td></tr>
<tr><td></td><td>1</td><td>1</td><td>3,38</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1,33</td></tr>
<tr><td>2</td><td></td><td></td><td>1,10</td></tr>
<tr><td></td><td>2</td><td></td><td>2,35</td></tr>
<tr><td>2</td><td>1</td><td></td><td>0,89</td></tr>
<tr><td>1</td><td>2</td><td></td><td>1,14</td></tr>
<tr><td>3</td><td></td><td></td><td>0,73</td></tr>
<tr><td></td><td>3</td><td></td><td>1,57</td></tr>
<tr><td>2</td><td></td><td>1</td><td>1,01</td></tr>
</table></td></tr>
<tr><td></td><td></td><td></td><td>R127</td><td>Gate pull-down resistor</td><td>During power-off, R127 ensures that the gate is tied to x_0V potential and the IGBT is turned off.</td></tr>
<tr><td></td><td></td><td></td><td>C68</td><td>External gate capacitor</td><td>External gate capacitance stabilizes the gate voltage. Gate's internal equivalent capacitance dominates the external gate capacitor.</td></tr>
<tr><td>Gate Soft Turn-off (GST) for U_LO_G</td><td>Control board of 70CVB0197 9, connector X17</td><td>On state:17mA current sink / off state: high impedance

Reference: DC-</td><td>H5</td><td>Provides functional isolation for GST signal</td><td>Has about 0,5A max output current for both source and sink</td></tr>
<tr><td></td><td></td><td></td><td>R62, C19</td><td>Needed to filter differential mode noise from GST signal</td><td>Capacitor value should be kept as small and resistor value as large as possible for not to cause extra delay to IGBT switching</td></tr>
</table>

FUNCTION	CONTROLLED BY	SIGNAL LEVELS / REFERENCE POINT	RELATED COMPONENTS	COMPONENT FUNCTION	NOTES
			R16, R18	Resistors are for filtering common mode noise from GST signal	The resistance should not be increased to maintain 17 mA current during on-state (~12 mA to optocoupler)
			C43, C76	Supply filter capacitors for optocoupler	
			R118, R119	Base current limiting for the signal blocking transistors	The resistors limit the base current of V31 and V32 to a reasonable value. The GST signal should only last for couple of milliseconds at maximum. During normal operation no current is going through these resistors. They have to be derated according to their peak pulse power. Tested setup had 150 Ohm resistors assembled. This leads to almost 6 W peak power and ~200 mA base current, which could be significantly decreased without affecting the functionality. The resistors should be replaced by 1…2.2 kOhm resistors (10…30 mA base current, 300…840 mW peak power for resistors).
			V31, V32	Signal blocking transistors	When GST is active, transistors V31 and V32 are switched on to ensure that normal gate driving signals from optocoupler are not allowed to pass. V32 ties predriver's input to -15 V, ensuring that turn-on half of the driver does not get drive signal. V31 ties predriver's turn-off side to -15 V, which ensures that driver's turn-off transistor V33 does not get control signal and stays non-conductive. In tested setup V31 and V32 were FZT651 high-current transistors. Better performance with lower extra cost and PCB are need would be achieved by replacing them with faster SOT-23 signal transistors.
			R121, C21	RC-filter / Base current limitation for V25	The resistor limits the base current of V25. Tested setup had 150 Ohm resistors assembled. This leads to almost 6 W peak power and ~200 mA base current, which could be significantly decreased without affecting the functionality. The resistors should be replaced by 1…2.2 kOhm resistors (10…30 mA base current, 300…840 mW peak power for resistors). Capacitor is used to filter noise from the base to prevent false activation of GST and to slow the start of gate discharging so that V31 and V32 have enough time to cut the driving signal before GST activation. Capacitor value should be kept low, but it may be possible to leave completely out. Before doing so, the behavior should be studied.
			V25, R92, C109	Gate Soft Turn-off (GST)	V25 switches on after the signal from driver's optocoupler to predriver and push-pull driver has been blocked. It ties the gate to -15 V through a GST resistor R92, causing the gate capacitance to discharge slowly when compared to normal turn-off. This significantly decreases the overvoltage peaks during turn-off after output phase short circuit. C109 is used to "kick-down" the gate voltage momentarily to 2,5 V to speed up the beginning of the turn-off process. The gate voltage recovers fast to a level of 10…12 V, depending on the value of R_{GST} (R92). The capacitance of C109 is dependent of the IGBT gate capacitance and the value of the external gate capacitor. Switching the gate to -15 V through C109 causes the IGBT to reach the top of a lossy, linear region. After this the remaining gate charge can be discharged slowly through R92, which causes the IGBT current slowly decrease to zero. C109 is dependent of external gate capacitor value and IGBT's gate capacitances. Using larger resistance lowers the peak of recovery voltage, but on the other hand allows the short circuit to be present in output longer. In tested setup 150 Ohms was regarded as a decent compromise between short circuit's duration and the amplitude of recovery voltage peak.

APPENDIX B: TABLE OF COMPONENTS' THERMAL LIMITS AND RECOMMENDED MAXIMUM TEMPERATURES

Component reference	Component type	Reference manufacturer	Absolute maximum temperature	Recommended maximum operating temperature, derated value	Maximum temperature with full power	Derating factor and limiting variable, commonly used in industry	Maximum power, datasheet value for lowest acceptable optional component	Maximum power at 70 °C, derated value
H4, H5	HCPL-J314	Avago Technologies	100 °C	80 °C	25 °C	80 % of maximum ambient temperature	600 mW (output power)	420 mW
C21, C22, C36, C43, C45, C68 C75, C76, C98, C99, C100, C101, C109	General purpose ceramic capacitor [GRM31xR7]	muRata	125 °C	100 °C	N/A	80 % of ambient temperature	N/A	N/A
R50, R95, R118, R119, R121, R122, R133	General purpose chip resistor, 0805 package [CRCW0805]	Vishay	155 °C	N/A[1]	70 °C	50 % of absolute maximum power	125 mW	62.5 mW
R45, R127, R147, R148	General purpose chip resistor, 1206 package [CRCW1206]	Vishay	155 °C	N/A[1]	70 °C	50 % of absolute maximum power	250 mW	125 mW
R2, R9, R90, R92, R96, R130, R131, R132	Pulse power resistant MELF resistor [MMB0207]	Vishay	155 °C	N/A[1]	70 °C	50 % of absolute maximum power	1.0 W	0.5 W
V31, V32, V35	FZT651	Zetex	150 °C	N/A[1]	25 °C	70 % of absolute maximum power	2.0 W	1.4 W
V36	FZT751	Zetex	150 °C	N/A[1]	25 °C	70 % of absolute maximum power	2.0 W	1.4 W
V25, V33	FZT851	Zetex	150 °C	N/A[1]	25 °C	70 % of absolute maximum power	2.0 W	1.4 W
V34	FZT951	Zetex	150 °C	N/A[1]	25 °C	70 % of absolute maximum power	2.0 W	1.4 W
V29	BAV99	ON Semiconductor	150 °C	N/A[1]	25 °C	70 % of absolute maximum power	250 mW	175 mW
V16, V27	BAV70	ON Semiconductor	150 °C	N/A[1]	25 °C	70 % of absolute maximum power	250 mW	175 mW
V14, V30	BAW56	ON Semiconductor	150 °C	N/A[1]	25 °C	70 % of absolute maximum power	250 mW	175 mW

[1] = Derating according to power loss

APPENDIX C: EFFECT OF MISSING KELVIN EMITTER

During measurements, it was noticed that low-side IGBT was continuously producing higher switching losses than expected. First random causes had been marked off from reasons for such behavior by changing the used IGBT modules and the driver board. Since the losses were still at a higher level than expected, decreasing the resistance of turn-on resistors and increasing supply voltages was tried with only a limited effect on the losses.

After examining the IGBT module's internal layout in Figure C.1, it was found out that the high-side IGBT has an additional pad for the gate signal's reference voltage, which is the output phase for the high-side IGBT. The pad was routed separately from the IGBT's emitter, causing no working current to conduct in the bonding wire connecting the additional reference pad to the emitter. The low-side IGBT does not have a separate pad for the reference voltage, which in low-side IGBT's case is DC-. Furthermore, the gate reference pin on the IGBT module's casing is connected to the DC- bus, instead of connecting it straight to the IGBT's emitter. The low-side IGBT is located on another copper plate than the DC- bus, and the plates are connected by bonding wires. The equivalent circuit is included in Figure C.2. When the IGBT or the free-wheeling diode is loaded, the low-side load current will conduct between the plates via the bonding wires and cause a voltage loss over them. This voltage loss is increasing the potential of the IGBT's emitter in relation to DC-, which makes the control voltage from the gate to the emitter to decrease. Having a lower gate voltage causes higher losses during both switching and conduction state. Semikron is going to be contacted for this issue.

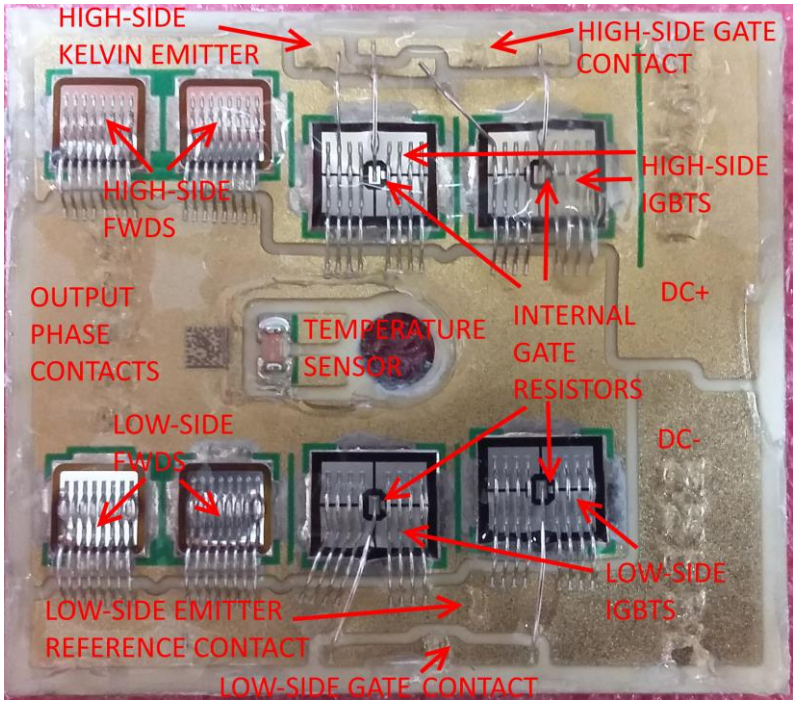

Figure C.1: Picture of Semikron SKiiP 24GB12T4V1 internal structure

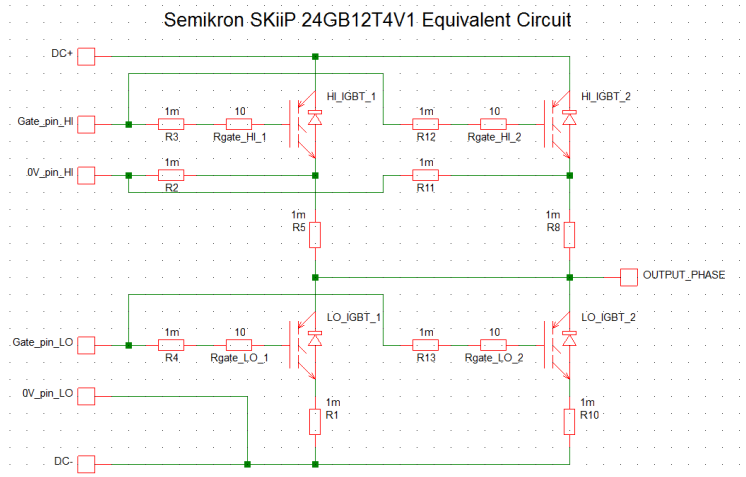

Figure C.2: Equivalent circuit of the Semikron SKiiP 24GB12T4V1 IGBT module. The bond wires are drawn as 1m resistors, although they represent mainly inductive stray components during switching.

Table C.1: Oscilloscope setup in measurement. The test points refer to the U_LO driver schematics found on pages 2 and 3 in Appendix J.

Oscilloscope Channel	**Point of measurement**	**U_LO**	**V_HI**	**REFERENCE** DC- = PE
CH3	IGBT's collector-emitter voltage	TP45 -> TP43	TP44 -> TP46	N/A
CH4	IGBT's collector current	N/A	N/A	N/A
CH1	Turn-on / turn-off driver transistor's collector	TP124 / TP132	TP63 / TP67	x_ 0V
CH2	IGBT's gate	TP138	TP12	x_ 0V
Math 1	Switching power loss, CH3 * CH4	N/A	N/A	N/A

Figure C.3: The turn-on switching energy of V_HI IGBT with a 150 A load current and 600 V DC link voltage. Time scale is 100 ns/div.

Figure C.4: The turn-on switching energy of U_LO IGBT with a 150 A load current and 600 V DC link voltage. Time scale is 250 ns/div.

As can be seen from the Figures C.3 and C.4 the main circuit waveforms are significantly different. Measurements were performed with oscilloscope setup of Table C.1. The gates are controlled with a similar voltage curve. In curves of V_HI in Figure C.3, the increased gate voltage causes a dip of 115 V during the following 50 ns time interval. The first step is followed by a flat section in the curve for another 50 ns. After that, a sharp knee can be seen to appear, bending the voltage curve steeply towards zero. Meanwhile, the load current increases almost linearly to a peak value of ~250 A, and then decreases to a level of ~150 A. The calculated curve, Math 1, indicating the energy loss of IGBT during switching event, has a clear peak simultaneously with the peak in current waveform. The switching event lasts for 186 ns and the calculated switching energy is 9,754 mJ.

When the turn-on waveforms of U_LO in Figure C.4 are observed, it can be seen that the transitions of IGBT's collector current and collector-to-emitter voltage are not as fast as for V_HI. The V_{CE} curve has a drop of 60 V after the voltage on the IGBT module's gate pin has increased to its final value. The collector current starts to increase rapidly but after ~50 ns the slope decreases significantly. Simultaneously with the change in the slope, VCE starts to increase back towards the value of DC link. This is caused by a voltage loss in the bonding wires between DC- bus and IGBT chip, which again causes a decrease in the IGBT's internal gate-emitter voltage and therefore also limits the control of the IGBT. When the IGBT module's internal RC-filter, formed by internal gate resistor and gate capacitance, slowly allows the real gate voltage to increase to a value that no longer limits the IGBT current, V_{CE} starts to fall. This can be seen in the waveforms as a second knee on the I_C and V_{CE} curves. When the collector current has reached the level of ~170 A, the slope sets as zero and V_{CE} starts to fall linearly towards zero. The turn-on event lasts for 393 ns and has a switching energy of 23,32 mJ, which is 239 % when compared to the turn-on energy of V_HI.

APPENDIX D: MAIN CIRCUIT SWITCHING WAVEFORMS

The results from measurements done to find out the IGBT's switching behavior with the studied driver are included in this appendix. The measurements were conducted for the final driver assembly with the oscilloscope channel setup of Table D.1. The ambient temperature during measurements was varied by installing the IGBT heat sink plate on a temperature controlled heat plate. The driver circuit's temperature was confirmed to stay below 60 °C with a thermal imager.

Table D.1: Setup in measurement. The test points refer to the U_LO driver schematics found on page 3 in Appendix J.

Oscilloscope Channel	**Point of measurement**	**V_HI**	**REFERENCE** DC- = PE
CH3	IGBT's collector-emitter voltage	TP44 -> TP46	N/A
CH4	IGBT's collector current	N/A	N/A
CH2	IGBT's gate voltage	TP12	V_HI_ 0V
Math 1	Switching power loss, CH3 * CH4	N/A	N/A

Figure D.1: Turn-on switching loss with 600 V DC link voltage and 150 A load current at 25 °C IGBT heatsink temperature.

Figure D.2: Turn-on switching loss with 600 V DC link voltage and 150 A load current at 85 °C IGBT heatsink temperature.

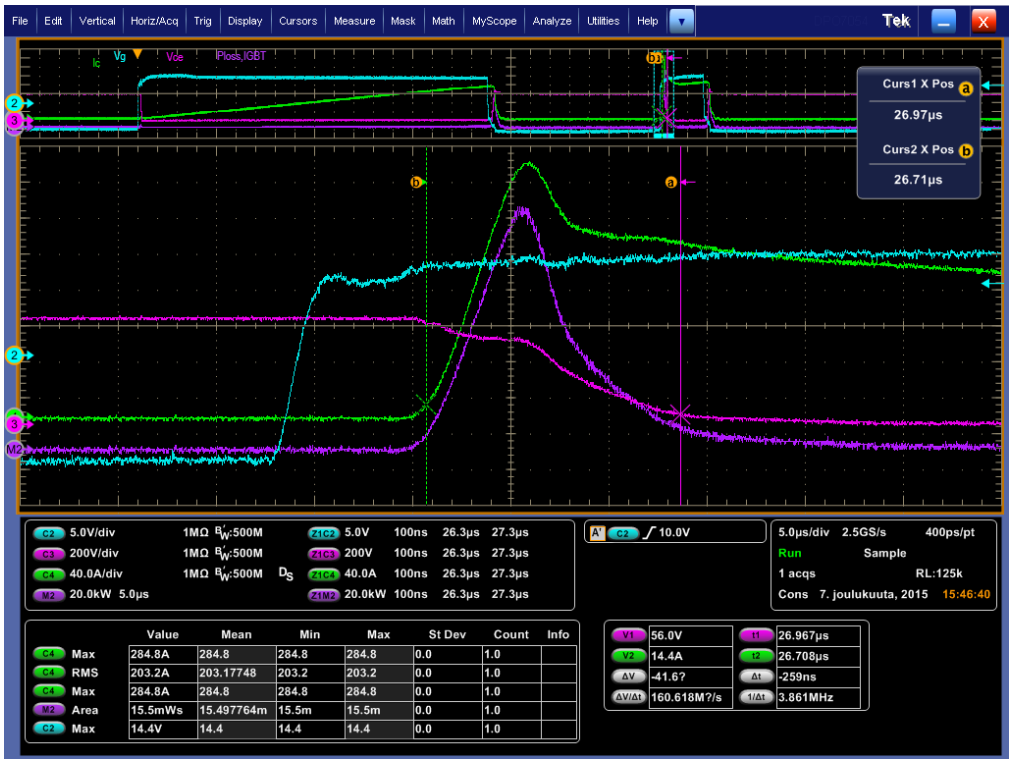

Figure D.3: Turn-on switching loss with 600 V DC link voltage and 150 A load current at 150 °C IGBT heatsink temperature.

Figure D.4: Turn-on switching loss with 900 V DC link voltage and 150 A load current at 25 °C IGBT heatsink temperature.

Figure D.5: Turn-off switching loss with 600 V DC link voltage and 150 A load current at 25 °C IGBT heatsink temperature.

Figure D.6: Turn-off switching loss with 600 V DC link voltage and 150 A load current at 85 °C IGBT heatsink temperature.

Figure D.7: Turn-off switching loss with 600 V DC link voltage and 150 A load current at 150 °C IGBT heatsink temperature.

Figure D.8: Turn-off switching loss with 900 V DC link voltage and 150 A load current at 25 °C IGBT heatsink temperature.

APPENDIX E: OPERATION OF GATE SOFT TURN-OFF WITH R_{GST} AND C_{GST} VARIATION

The results from measurements done to find out the optimal values for soft turn-off resistor and capacitor are included in this appendix. The measurements were conducted for the final driver assembly with oscilloscope setup of Table E.1 and hardware setup of Table E.2. The ambient temperature during measurements was 25 °C. Normal turn-off is included as a reference. 1,5 µH load coil was used to simulate a type I hard short circuit.

Table E.1: Oscilloscope channels in gate soft turn-off measurements. The test points refer to the U_LO driver schematics found on page 3 in Appendix J.

Oscilloscope Channel	**Point of measurement**	**V_HI**	**REFERENCE** DC- = PE
CH3	Voltage over IGBT, Vce	TP44 -> TP46	N/A
CH4	Current through IGBT's DC+ bus	N/A	N/A
CH2	IGBT's gate	TP12	V_HI_0V

Table E.2: Hardware setup in gate soft turn-off measurements.

PARAMETER	**VALUE**
DC-link voltage	600 V
Load current	520 A
Load inductance	1,5 µH
Pulse 1	4 us
Interval between pulses	9 us
Pulse 2	10 us
Snubber capacitors	Not assembled
Normal turn-off cancellation delay capacitor (between V54:base and V54:emitter)	0 nF
Capacitance of C_{GST} (C106) during R_{GST} variation measurements	10 nF
Resistance of R_{GST} (R55) during C_{GST} variation measurements	100 R
GST transistor delay capacitor C13	0 nF

Figure E.1: Reference turn-off with 600 V DC link voltage, load current of 520 A, without snubbers or GST. Peak voltage = 1,192 kV.

Figure E.2: Soft turn-off with 600 V DC link voltage and load current of 520 A but without snubbers. GST resistor R55 = 33 Ohm. GST capacitor C106 = 10 nF. Peak voltage = 1,048 kV.

Figure E.3: Soft turn-off with 600 V DC link voltage and load current of 520 A but without snubbers. GST resistor R55 = 56 Ohm. GST capacitor C106 = 10 nF. Peak voltage = 920 V.

Figure E.4: Soft turn-off with 600 V DC link voltage and load current of 520 A but without snubbers. GST resistor R55 = 100 Ohm. GST capacitor C106 = 10 nF. Peak voltage = 792 V.

Figure E.5: Soft turn-off with 600 V DC link voltage and load current of 520 A but without snubbers. GST resistor R55 = 150 Ohm. GST capacitor C106 = 10 nF. Peak voltage = 704 V.

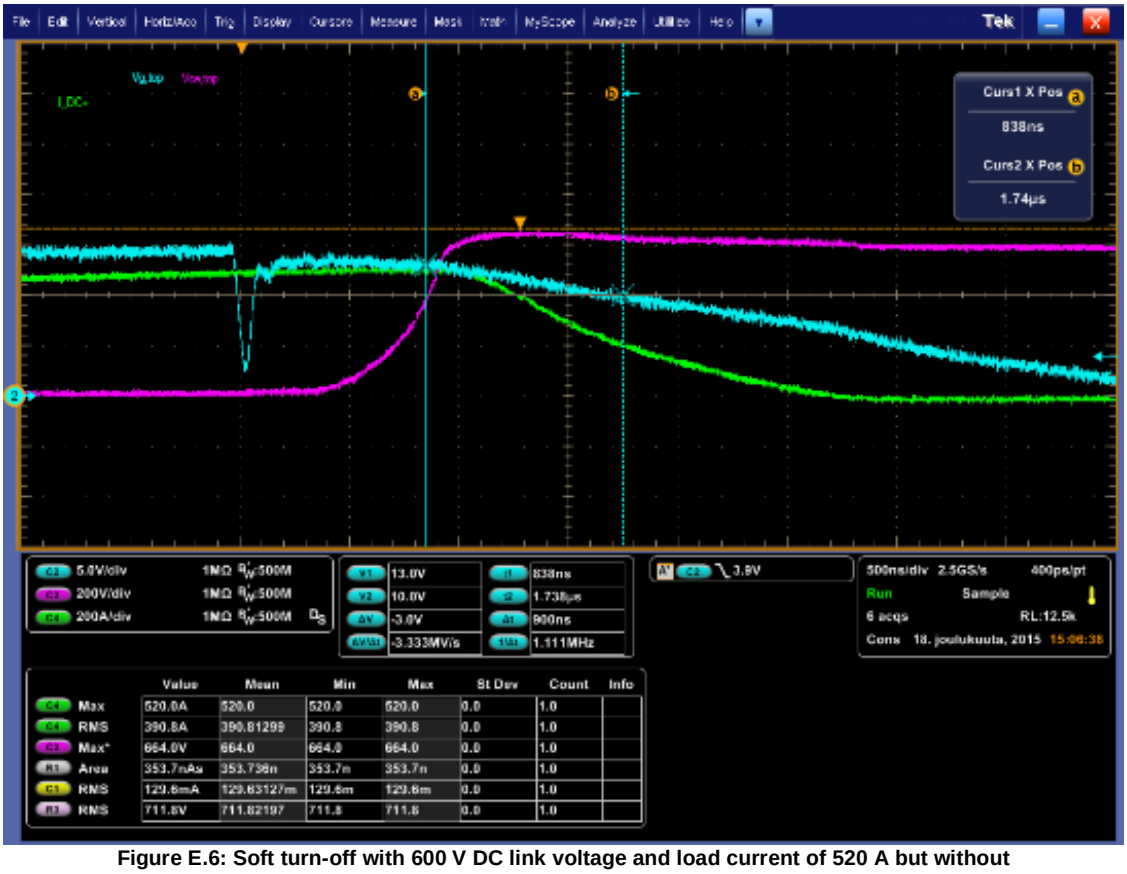

Figure E.6: Soft turn-off with 600 V DC link voltage and load current of 520 A but without snubbers. GST resistor R55 = 220 Ohm. GST capacitor C106 = 10 nF. Peak voltage = 664 V.

Figure E.7: Soft turn-off with 600 V DC link voltage and load current of 520 A but without snubbers. GST resistor R55 = 100 Ohm. GST capacitor C106 = 0 nF. Peak voltage = 768 V.

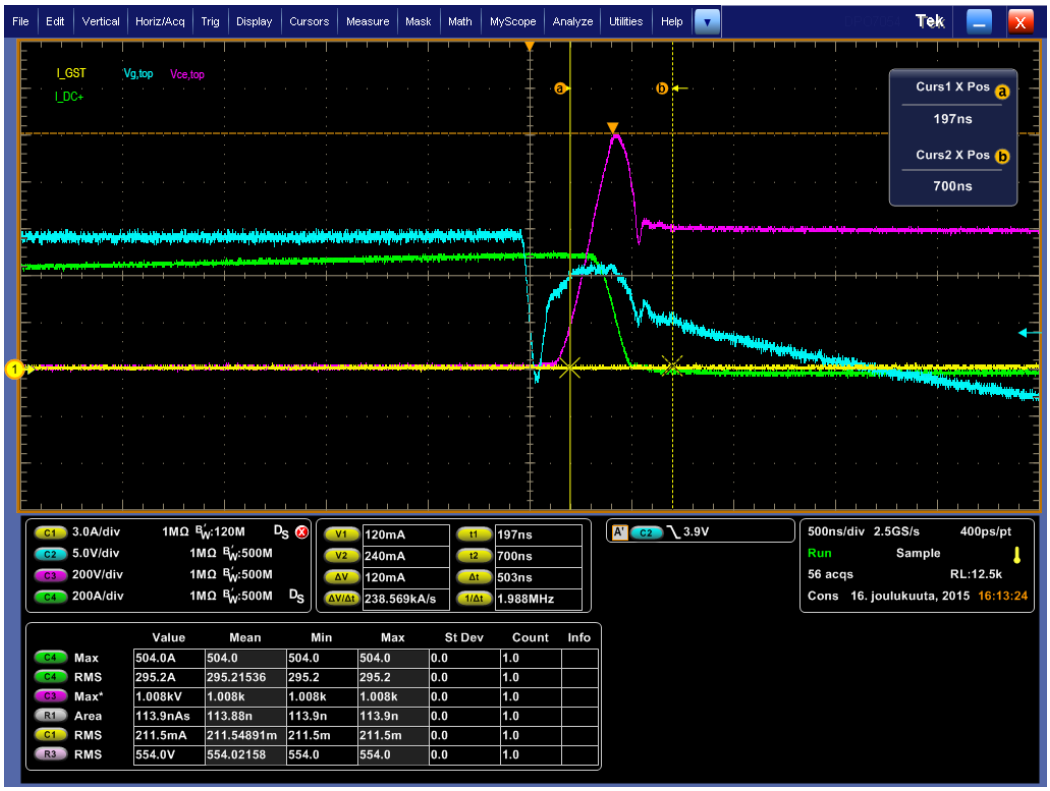

Figure E.8: Soft turn-off with 600 V DC link voltage and load current of 520 A but without snubbers. GST resistor R55 = 100 Ohm. GST capacitor C106 = 22 nF. Peak voltage = 1008 V.

APPENDIX F: OPERATION OF GATE SOFT TURN-OFF CIRCUIT WITH THE FINAL ASSEMBLY

The results from measurements done to verify the effects of soft turn-off are included in this appendix. The measurements were conducted for the final driver and soft turn-off circuit assembly with oscilloscope channel setup of Table F.1 and hardware setup of Table F.2. The ambient temperature during measurements was 25 °C. Normal turn-off is included as a reference. 1,5 µH load coil was used to simulate a type I hard short circuit. For soft turn-offs, the DC-link voltage was increased to prove that by using GST function, the drive would survive from situations when normal turn-off would cause damage due to overvoltage.

Table F.1: Oscilloscope channels in gate soft turn-off measurements. The test points refer to the U_LO driver schematics found on page 3 in Appendix J.

Oscilloscope Channel	**Point of measurement**	**V_HI**	**REFERENCE** DC- = PE
CH3	Voltage over IGBT, Vce	TP44 ->	N/A
CH4	Current through IGBT's DC+ bus	N/A	N/A
CH2	IGBT's gate	TP12	V_HI_0V

Table F.2: Hardware setup in gate soft turn-off measurements.

PARAMETER	**VALUE**
DC-link voltage	600 / 700 / 800 V
Load current	900 A
Load inductance	1,5 µH
Pulse 1	4 us
Snubber capacitors	Not assembled
GST capacitor C106	10 nF
GST resistor R55	150 R

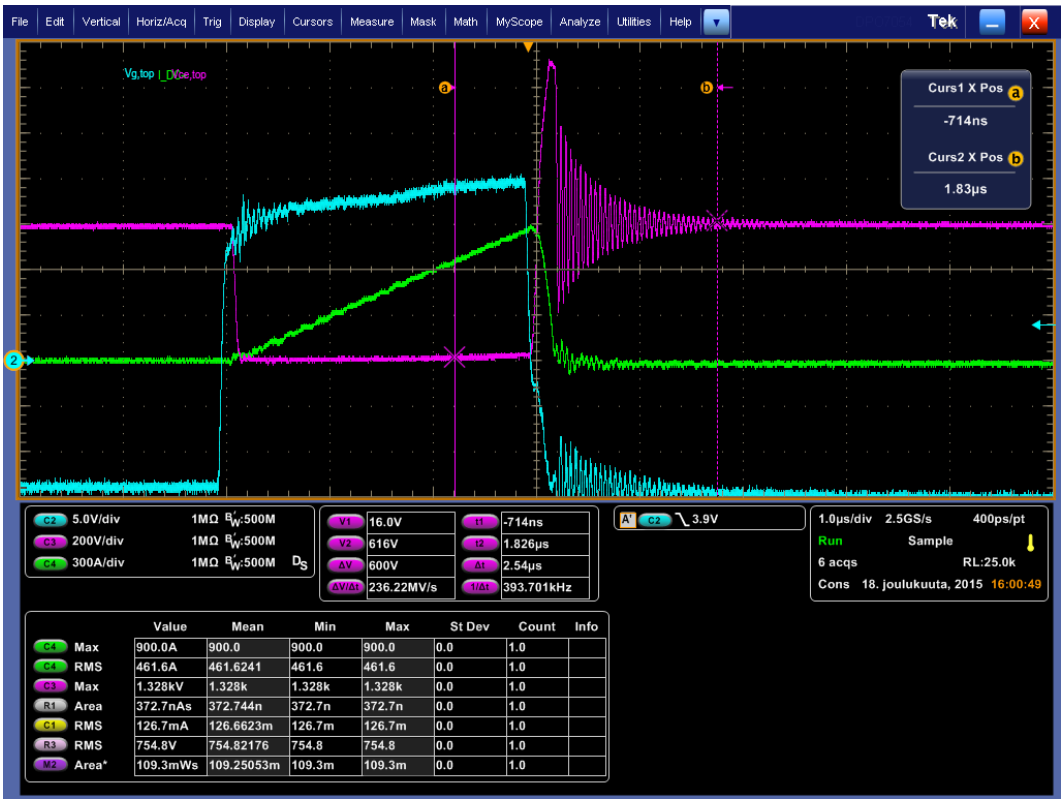

Figure F.1: Normal turn-off with 600 V DC link voltage and load current of 900 A but without snubbers. Peak voltage = 1,328 kV. Voltage increase during turn-off is 728 V.

Figure F.2: Soft turn-off with 700 V DC link voltage and load current of 900 A but without snubbers. GST resistor R55 = 150 Ohm. Peak voltage = 1,032 kV. Voltage increase during turn-off is 332 V.

Figure F.3: Soft turn-off with 800 V DC link voltage and load current of 984 A but without snubbers. GST resistor R55 = 150 Ohm. Peak voltage = 1,176 kV. Voltage increase during turn-off is 376 V.

APPENDIX G: EFFECT OF HIGH AMBIENT TEMPERATURE TO THE OPTOCOUPLER'S PROPAGATION DELAY

The results from measurements done to find out the effect of high ambient temperature to the delay of optocoupler HCPL-J314 are included in this appendix. During measurements the driver circuit was not yet adjusted but its influence for the behavior of optocoupler was considered insignificant. The ambient temperature during measurements varied by using a temperature controlled test cabin. Oscilloscope channel setup is introduced in Table G.1.

Table G.1: Oscilloscope setup in measurement. The test points refer to the U_LO driver schematics found on page 3 in Appendix J.

Oscilloscope Channel	**Point of measurement**	**V_HI**	**REFERENCE** DC- = PE
CH3	CPLD's pin	TP156	GND
CH1 (differential probe)	Voltage loss of optocoupler's input LED	TP18 -> TP14	N/A
CH4	Optocoupler's output	TP28	V_HI_0V

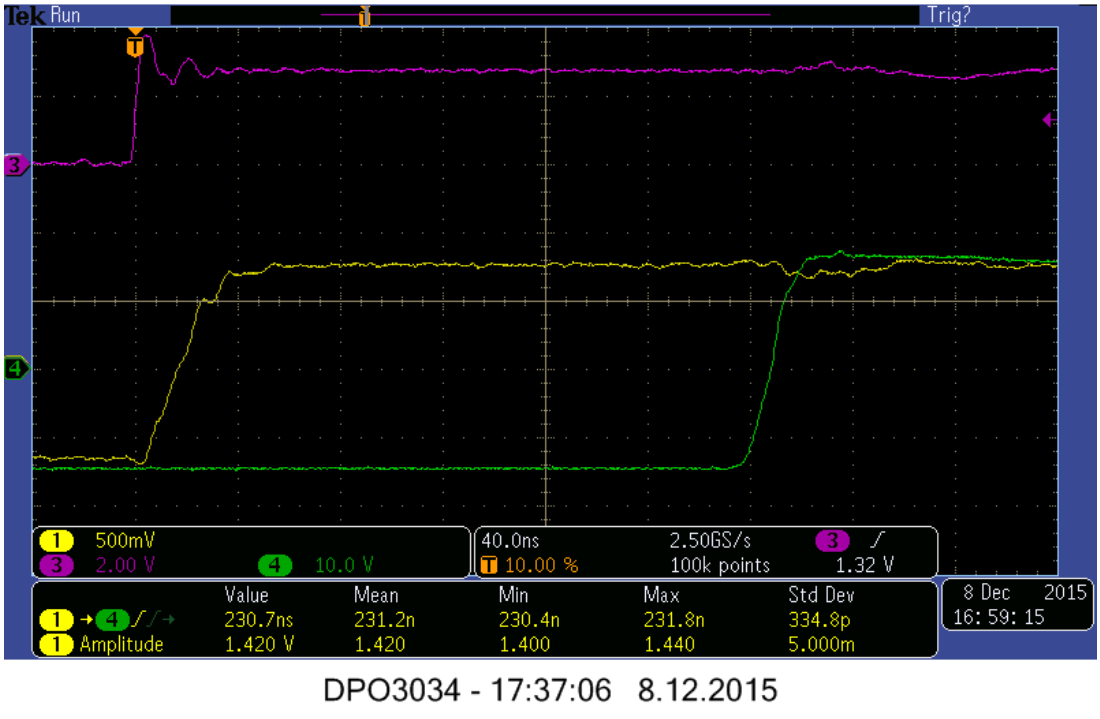

Figure G.1: The delay of HCPL-J314 optocoupler for turn-on in ambient temperature of 85 °C.

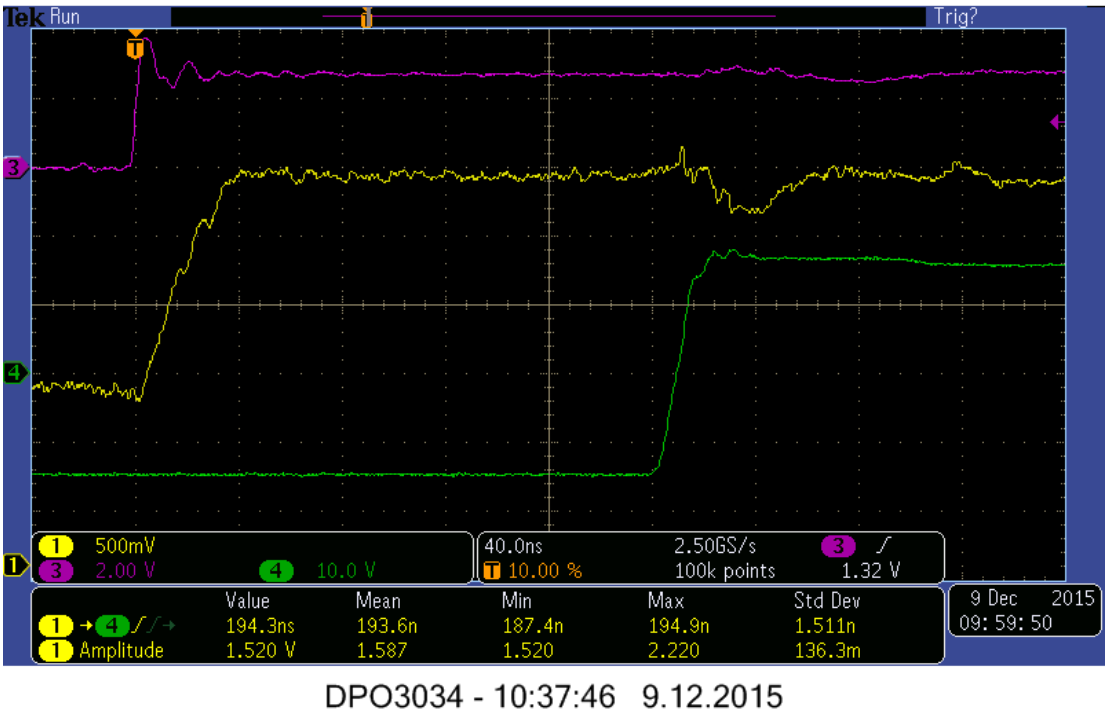

Figure G.2: The delay of HCPL-J314 optocoupler for turn-on in ambient temperature of 25 °C.

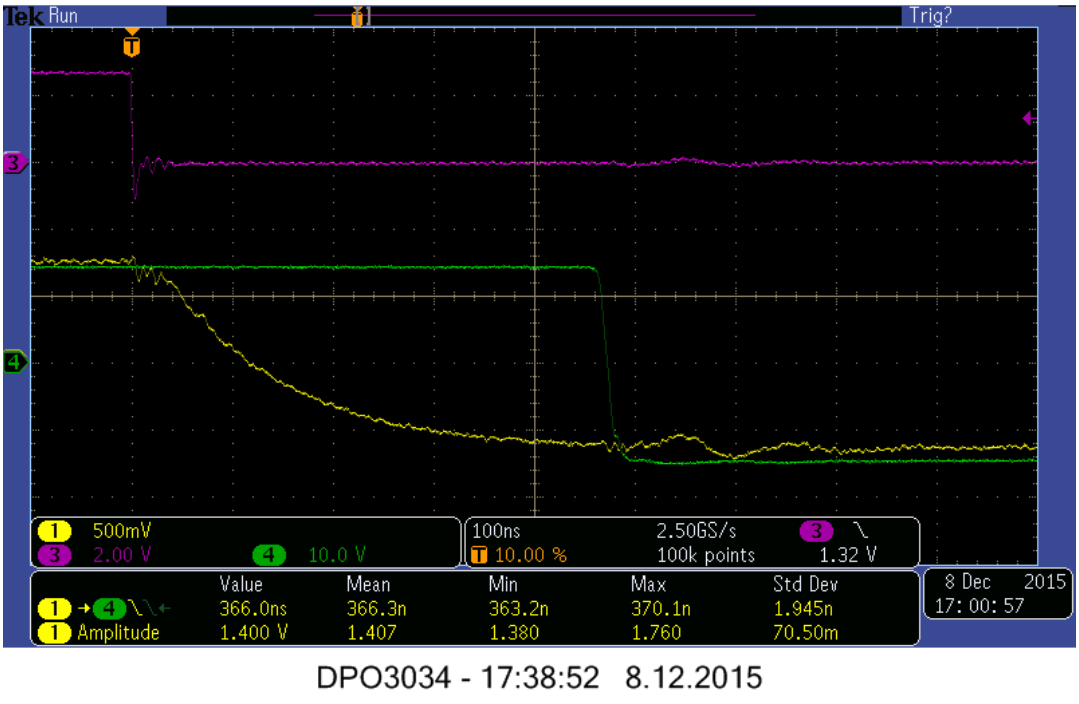

Figure G.3: The delay of HCPL-J314 optocoupler for turn-off in ambient temperature of 85 °C.

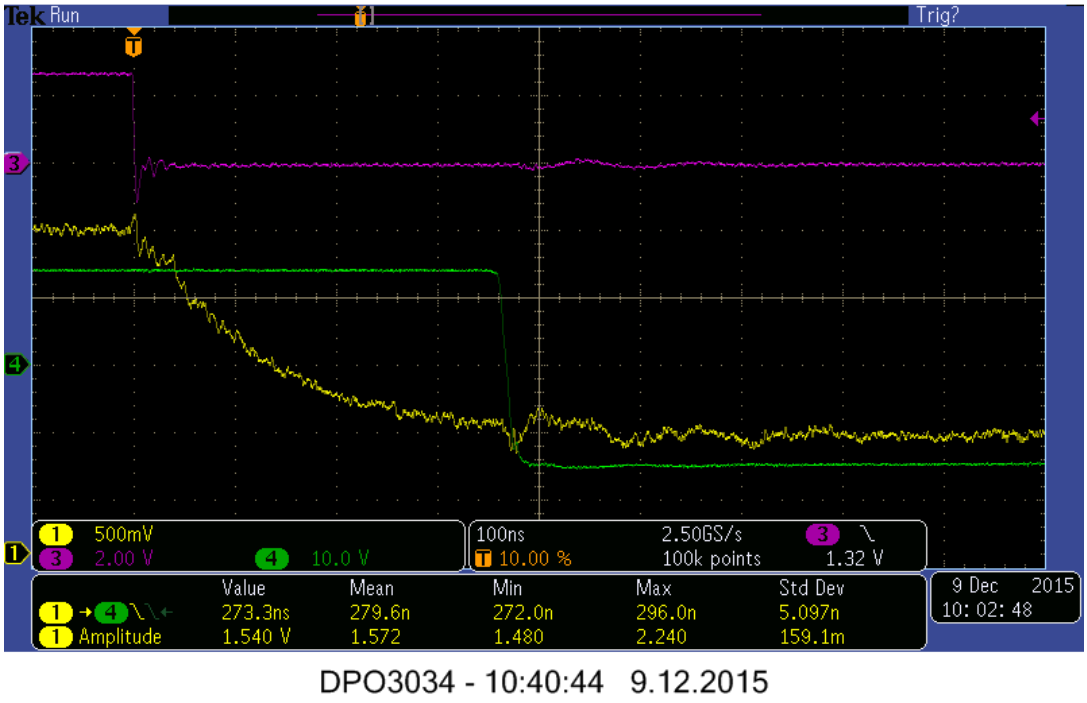

Figure G.4: The delay of HCPL-J314 optocoupler for turn-off in ambient temperature of 25 °

When comparing measured values of Figures G.1 – G.4 to the nominal values given in datasheet, it can be seen that for turn-on delays (T_{PLH}), the measured values are very close to the nominal values. For turn-off delays (T_{PHL}) the difference is relatively high, but still the effect of temperature increase is almost as expected. The difference can be partly explained with the difference in the test setup. For driving the input of the optocoupler, the manufacturer may use a switch that changes its state fast during switching. On the prototype, the input circuitry resembles a setup that is not recommended by the manufacturer. See Figure G.5 for details. [2]

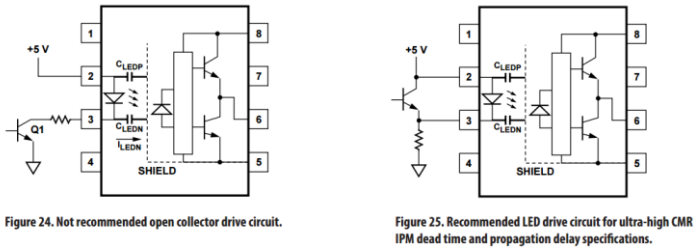

Figure 24. Not recommended open collector drive circuit.

Figure 25. Recommended LED drive circuit for ultra-high CMR IPM dead time and propagation delay specifications.

Figure G.5: Soft turn-off with 800 V DC link voltage and load current of 984 A but without snubbers. GST resistor R55 = 150 Ohm. Peak voltage = 1,176 kV. Voltage increase during turn-off is 376 V.

The used circuitry causes the input voltage to decrease slowly. Therefore defining the exact moment of turn-off signal for input is impossible or would need at least using a high-precision current measurement. The calculated delay value is using 50 % level of

the input voltage amplitude as a starting moment for the interval. The internal LED of optocoupler's input may already turn off earlier, which means that the true propagation delay would be longer than calculated. It should be considered using the input circuitry recommended by manufacturer. The results and nominal values are collected in Table G.2.

Table G.2: Oscilloscope channels in gate soft turn-off measurements.

	Nominal values, datasheet [ns]	**Measured values, mean [ns]**
T_{PLH} @ 25 'C	180	194
T_{PLH} @ 85 'C	220	231
T_{PHL} @ 25 'C	355	280
T_{PHL} @ 85 'C	430	366

The temperature coefficient for optocouplers' input forward voltage is -1,6 mV/'C. This means that in higher temperature, the LED in optocoupler's input will emit light with a lower input voltage. This causes he delay to slightly increase due to the presence of a capacitor in parallel with the input. Simultaneously the threshold level between logical high and low increases from 2,20 mA to 2,55 mA. This evens the effect out, but the change of forward voltage should be taken into account in the design by using a suitable current limiter.

APPENDIX H: OPERATION OF GATE DRIVER CIRCUIT AT 85 °C AMBIENT TEMPERATURE

The results from measurements done for the gate driver at 85 °C ambient temperature are included in this appendix. The purpose for these measurements was to verify that the temperature drift of the driver's semiconductors does not affect its performance significantly. Measurements were performed in a temperature controlled test cabin with oscilloscope channel setup of Table H.1.

Table H.1: Oscilloscope channels when measuring the driver circuit's behavior at ambient temperature of 85 °C. The test points refer to the U_LO driver schematics found on page 3 in Appendix J.

Oscilloscope Channel	Point of measurement	V_HI	REFERENCE DC- = PE
CH1	IGBT's gate	TP12	GND
CH2	Current through turn—on transistor's collector	N/A	N/A
CH3	CPLD pin	TP156	GND
CH4	Driver transistor's collector voltage	TP63	GND

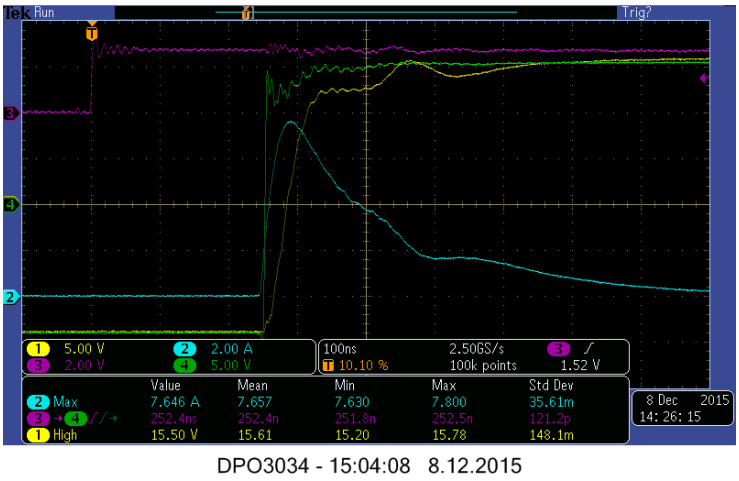

Figure H.1: Turn-on waveforms of V_HI driver without voltage on DC link. Ambient temperature is 85 °C.

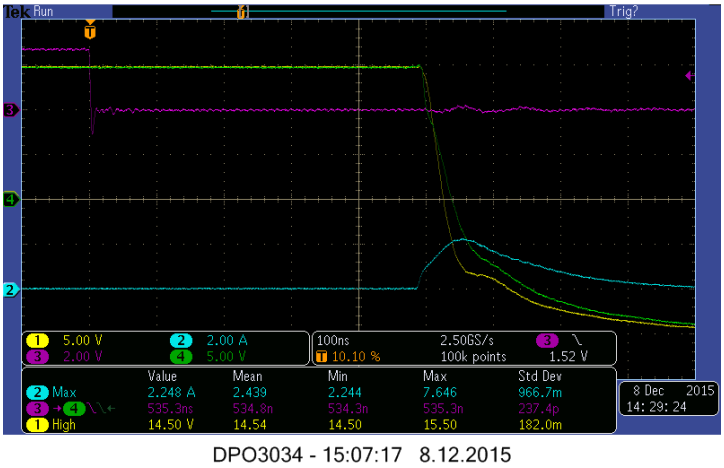

Figure H.2: Turn-off waveforms of V_HI driver without voltage on DC link. Ambient temperature is 85 °C.

APPENDIX I: GATE DRIVER SIMULATION SCHEMATICS (PSPICE)

The simulation schematics of the studied IGBT gate driver are included in this appendix. During development phase, some components were added or modified for better performance. The final driver schematics are included in Appendix J. R15 and C4 represent the IGBT module's internal gate resistor and approximated total gate capacitance. [15]

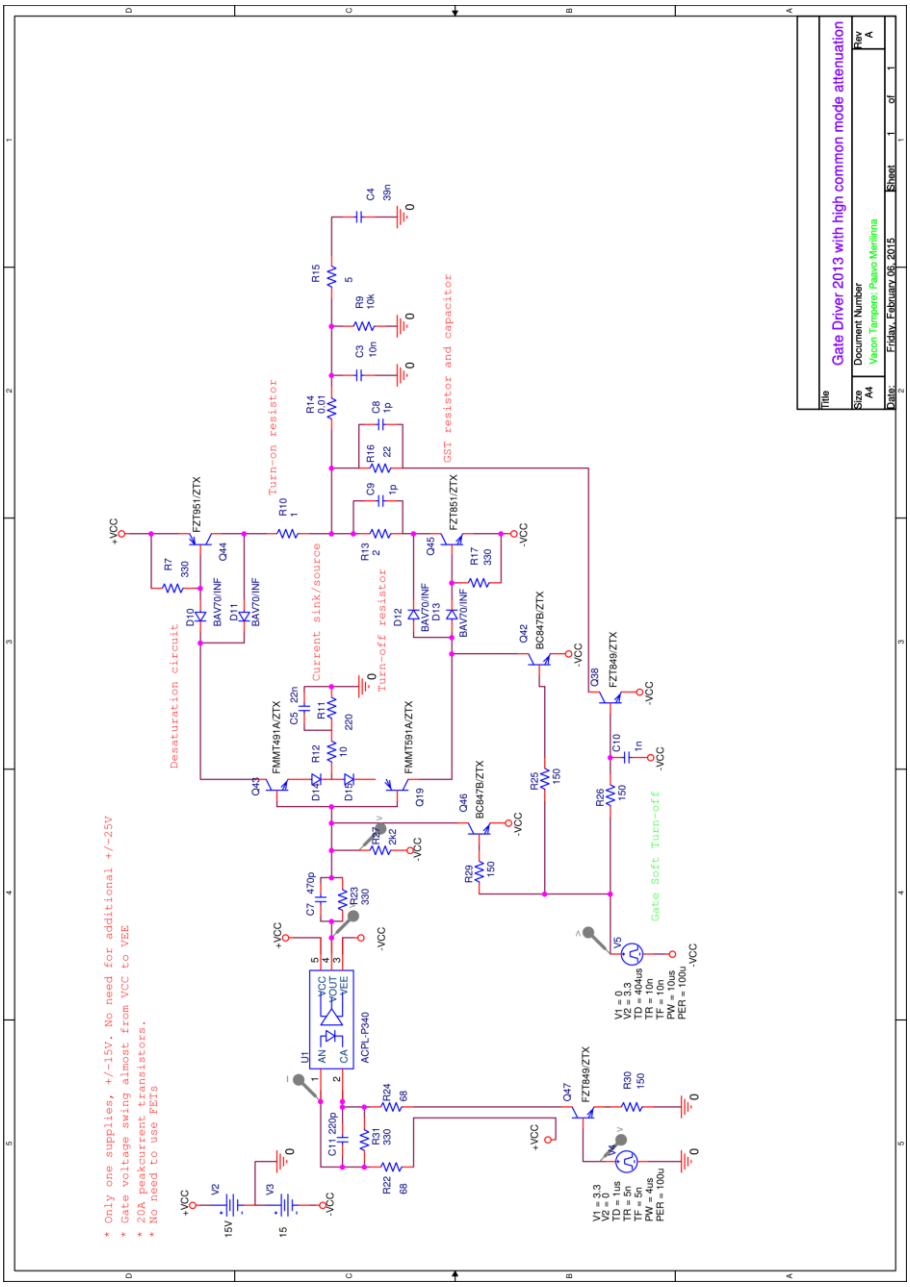

Figure I.1: Simulation schematics of the studied driver

APPENDIX J: GATE DRIVER SCHEMATICS (PADS)

The schematics of the studied IGBT gate driver are included in this appendix. On the prototyping board, there were four identical drivers assembled: U_LO, U_HI, V_LO and V_HI. Because the measurements were done mainly for U_LO and V_HI, only their schematics are included here. The schematics of the gate power supply was removed due to confidentiality.

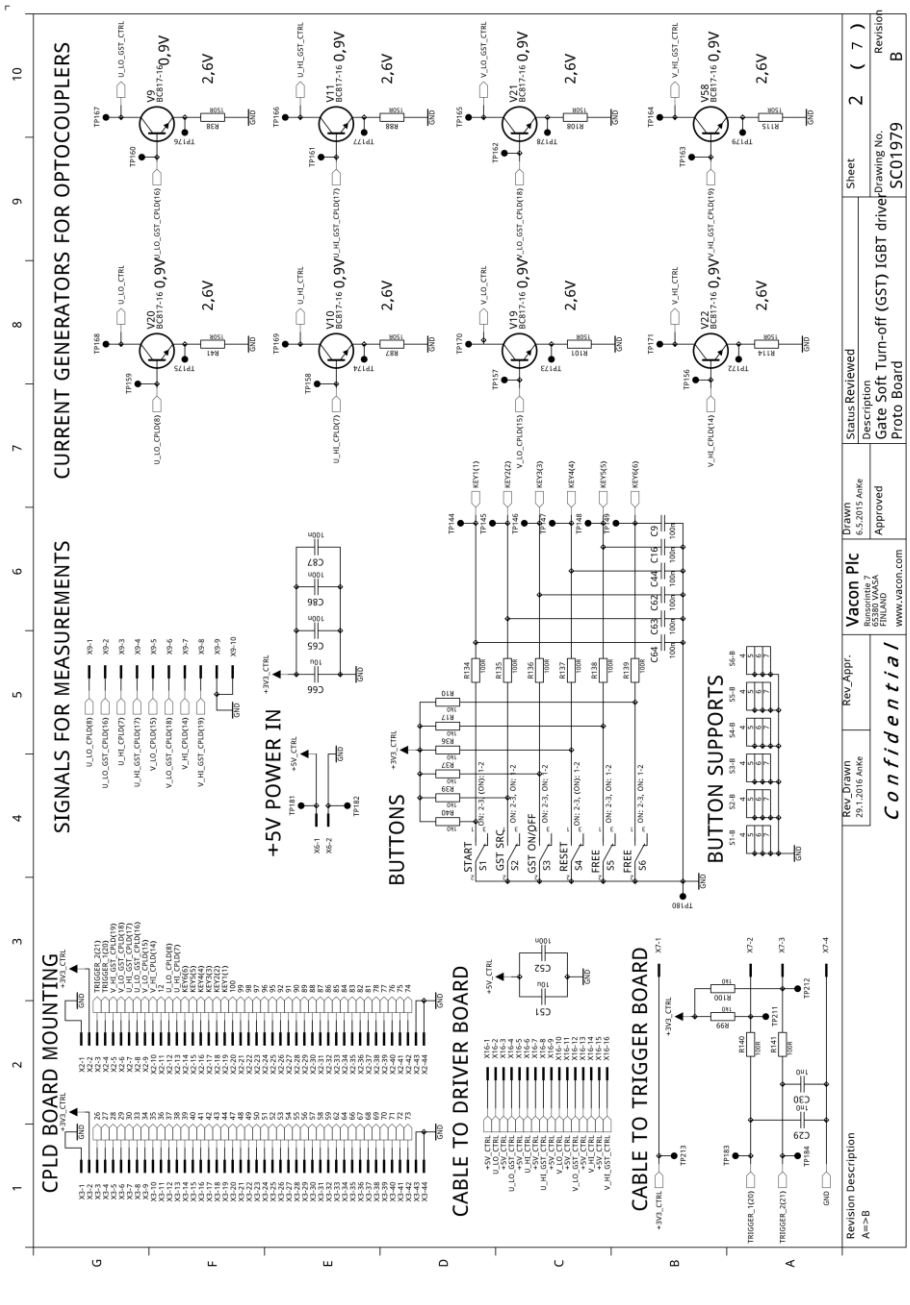

Figure J.1: Schematics of the driver prototyping board's control board section

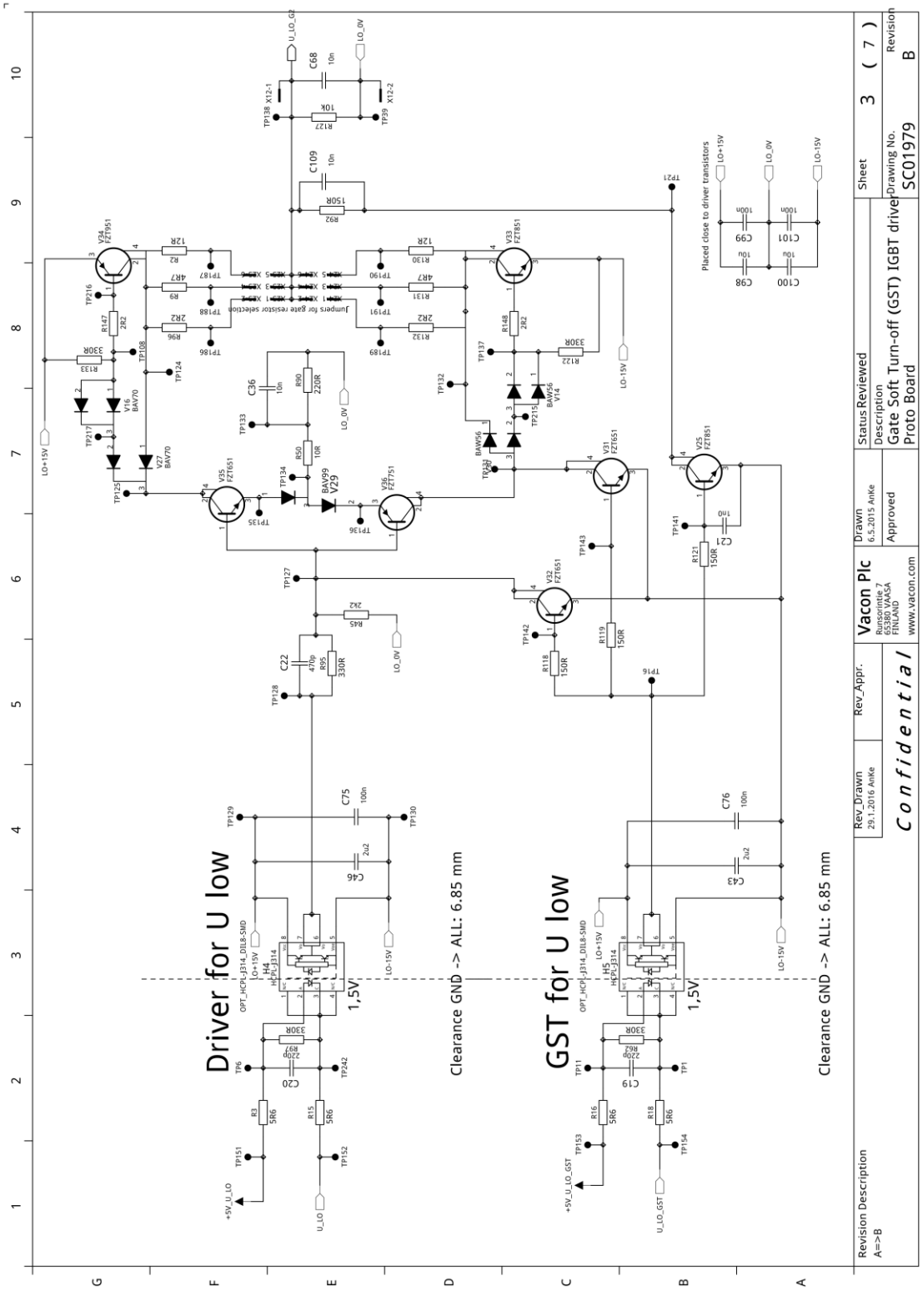

Figure J.2: Schematics of the driver prototyping board's U_LO driver channel

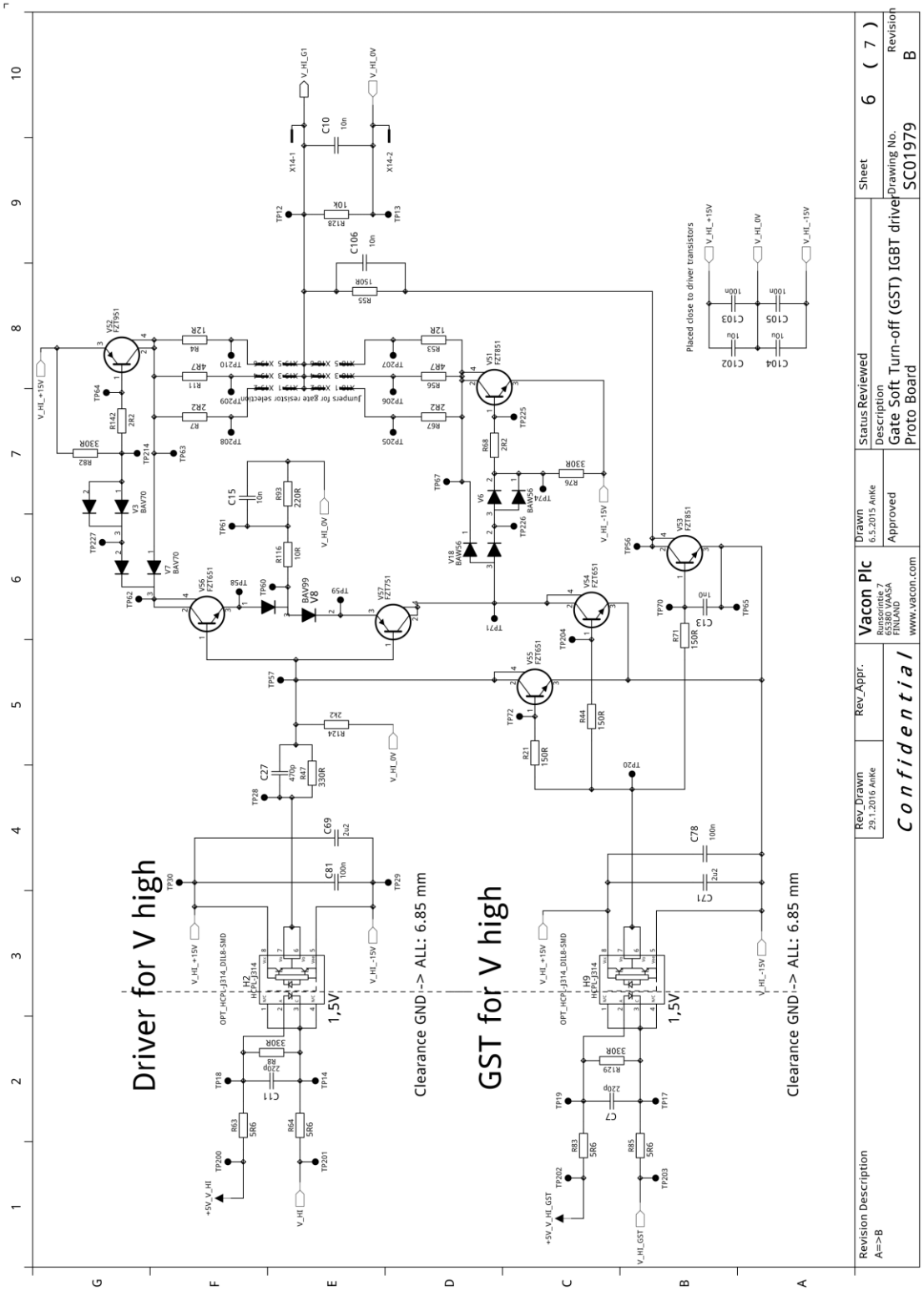

Figure J.3: Schematics of the driver prototyping board's V_HI driver channel

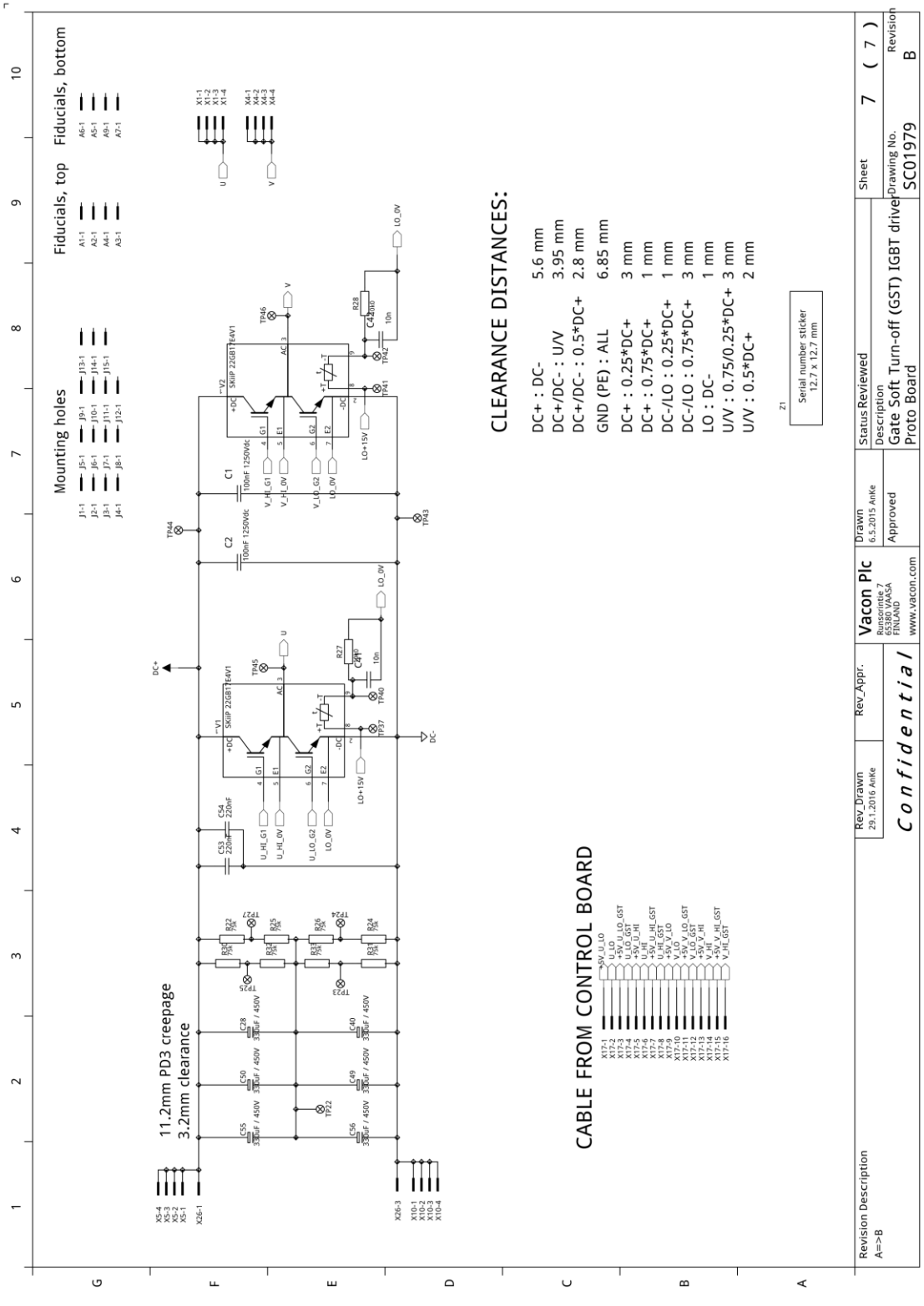

Figure J.4: Schematics of the driver prototyping board's main circuit and used isolation distances

APPENDIX K: GATE DRIVER LAYOUT IMAGES (PADS)

The layout images of the studied driver are included in this appendix. The layout was done in two-layer PCB with two-sided assembly. Copper areas are colored light gray. Component pads, traces and vias are colored dark gray.

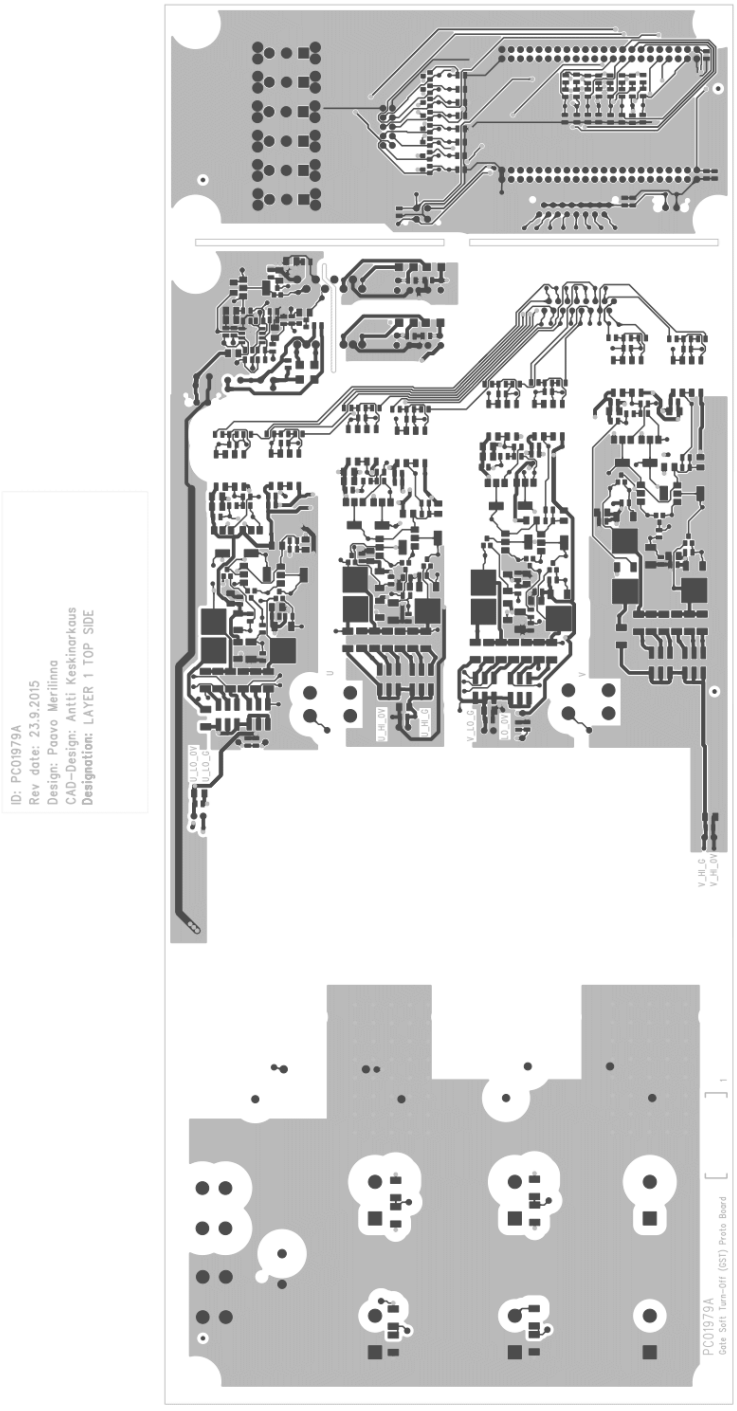

Figure K.1: Top-side layout image of the studied prototyping board (70CPE1979A)

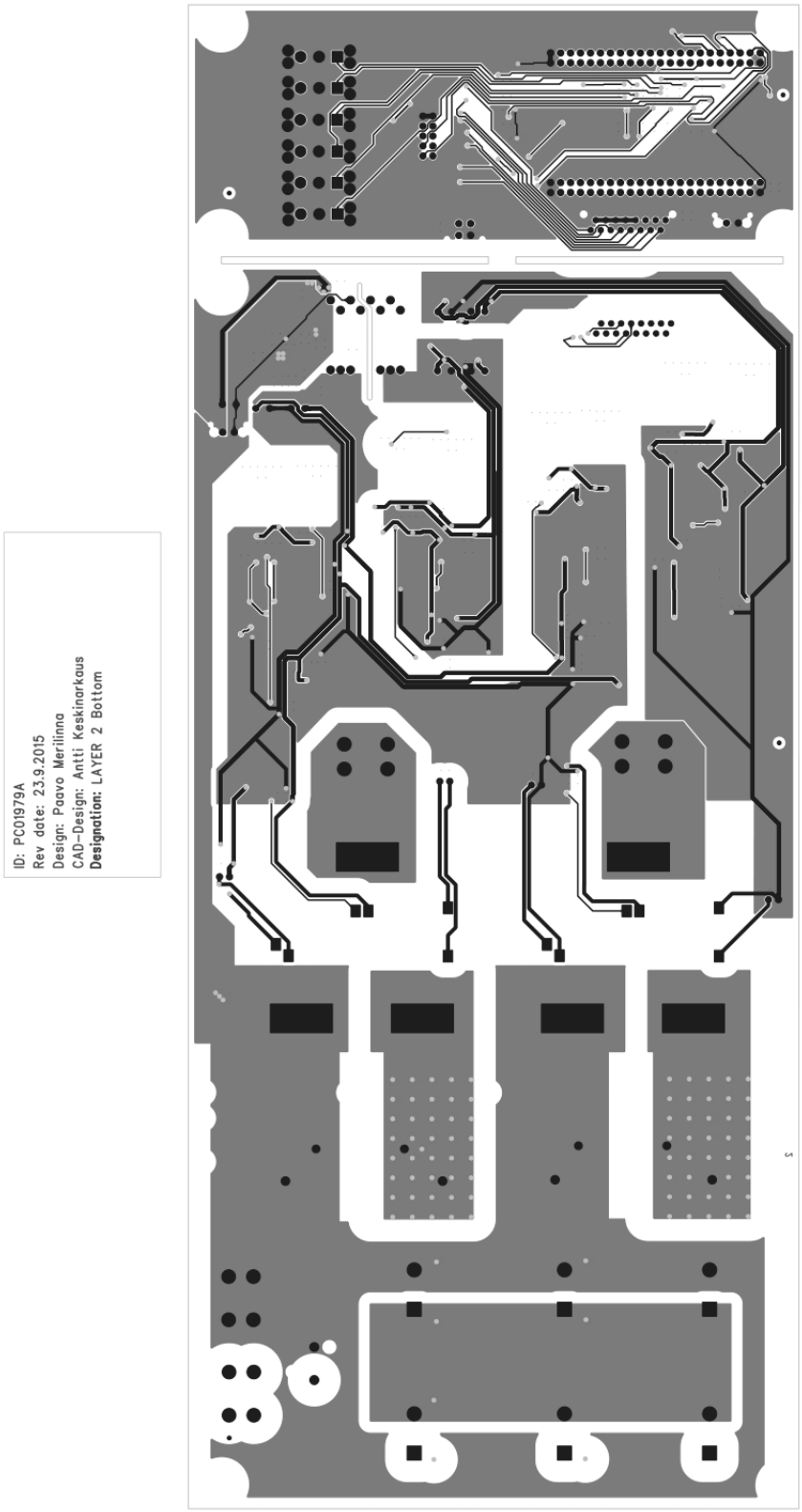

Figure K.2: Bottom-side layout image of the studied prototyping board (70CPE1979A)

APPENDIX L: GATE DRIVER ASSEMBLY IMAGES (PADS)

The assembly images of the studied driver are included in this appendix. The layout was done in two-layer PCB with two-sided assembly.

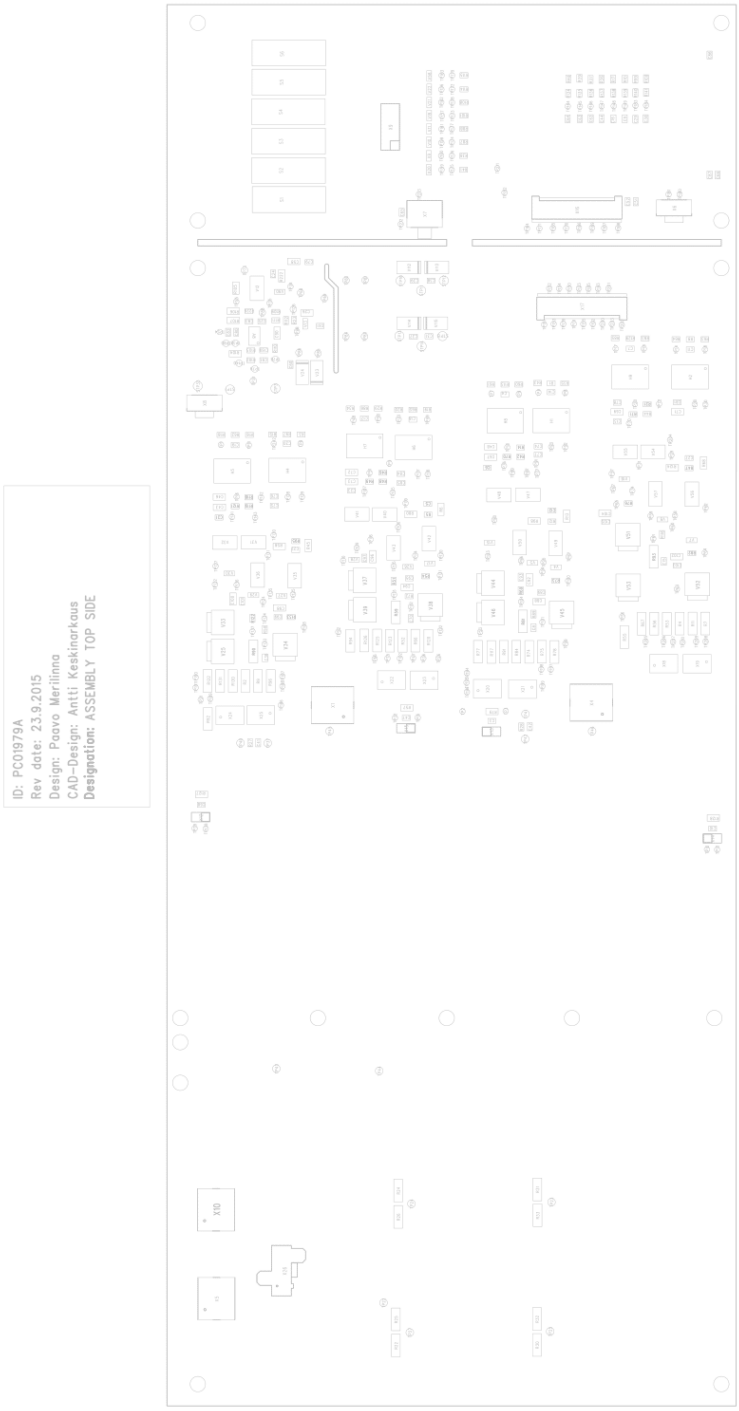

Figure L.1: Top-side assembly image of the studied prototyping board (70CPE1979A)

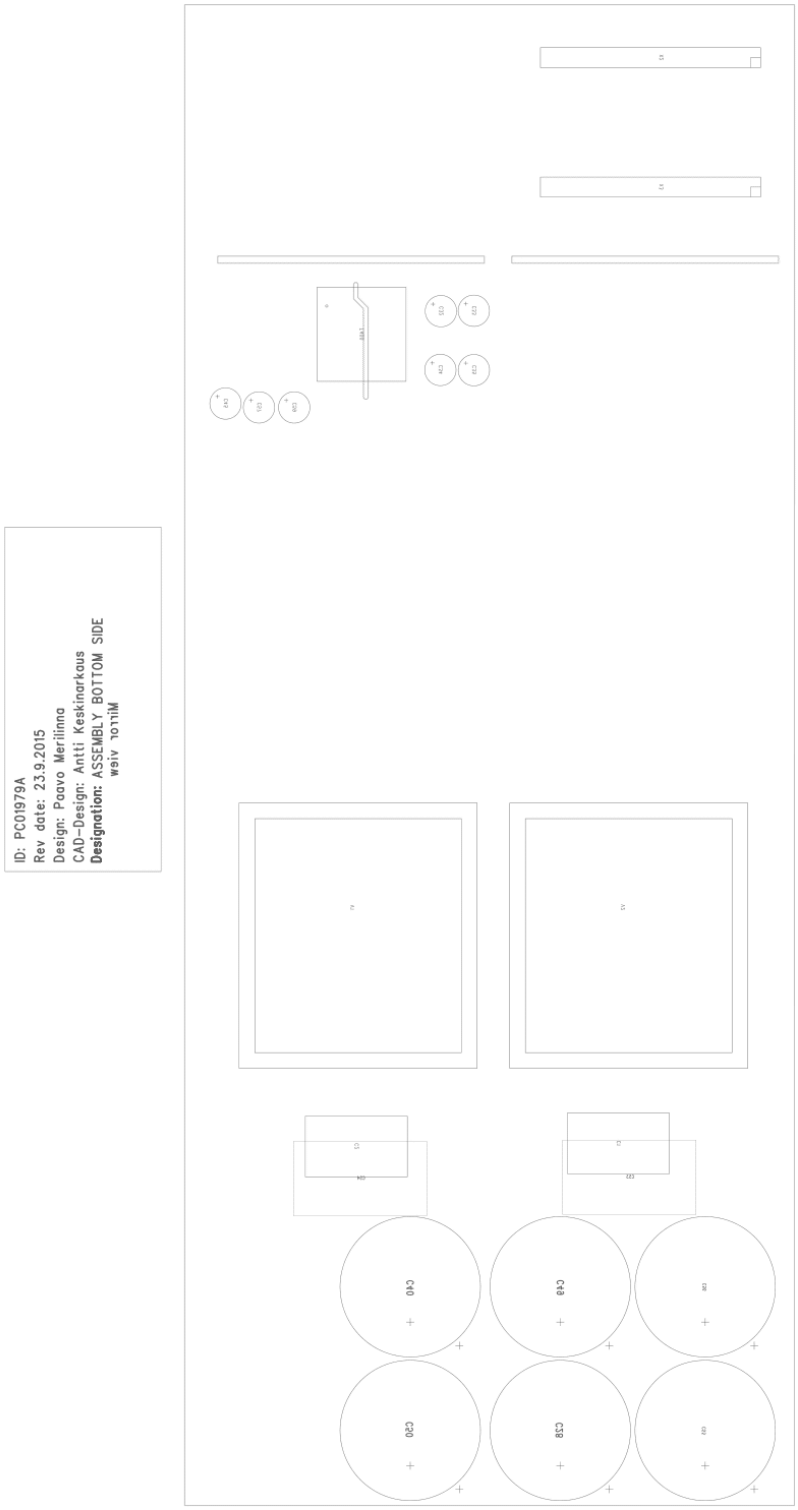

Figure L.2: Bottom-side assembly image of the studied prototyping board (70CPE1979A)

APPENDIX M: OPERATION OF THE REFERENCE DRIVER CIRCUIT

Results from measurements done for the reference gate driver at 25 °C ambient temperature are included in this appendix. The purpose for these measurements was to provide a comparison for the performance of the actual studied driver circuit. The same IGBT modules were used for the measurements. Also the main circuit layout and gate power supply were closely similar. Therefore the differences are caused by the driver circuit. Table M.1 presents the used oscilloscope setup.

Table M.1: Oscilloscope channels when measuring the reference driver circuit's behavior. The test points refer to the U_LO driver schematics found on page 3 in Appendix J.

Oscilloscope Channel	Point of measurement	V_HI	REFERENCE DC- = PE
CH1	Optocoupler's output	TP22	V_HI_0V
CH2	Gate pin	TP23	V_HI_0V
CH3	Driver's output, driver transistors' emitters	TP30	V_HI_0V
CH4	Current through gate resistor (gate current)	N/A	N/A

Figure M.1: Turn-on waveforms of reference V_HI driver with 600 V DC-link.

Figure M.2: Turn-off waveforms of reference V_HI driver with 600 V DC-link.

Figure M.3: Turn-on energy and main circuit waveforms of reference V_HI driver with 600 V DC-link.

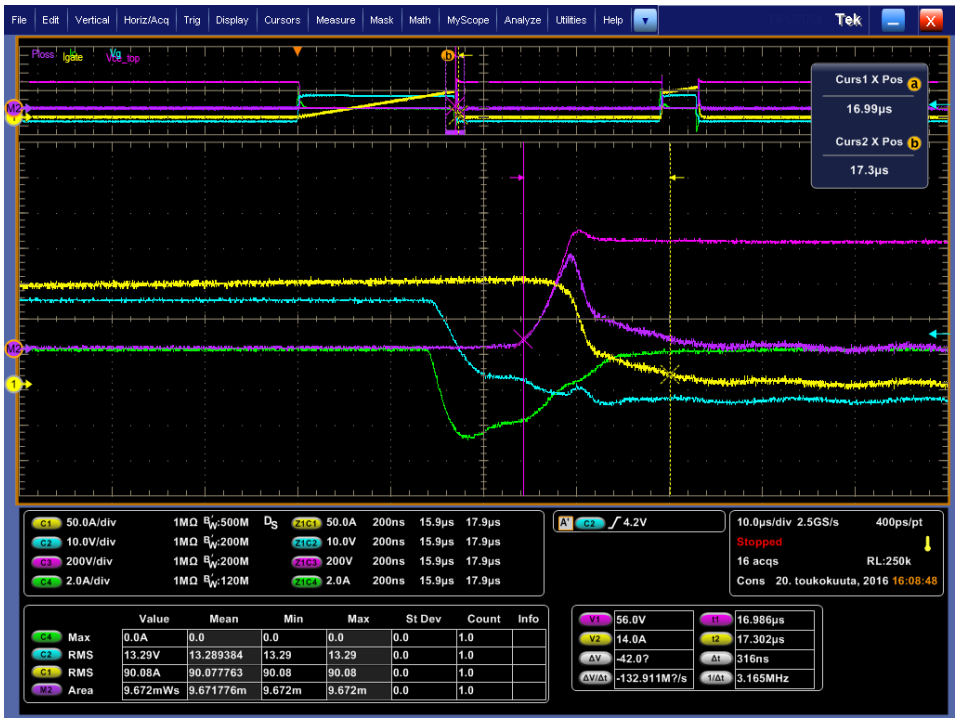

Figure M.4: Turn-off energy and main circuit waveforms of reference V_HI driver with 600 V DC-link.